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Potential-induced degradation: a challenge in the commercialization of perovskite solar cells

Hasan Raza,[a] Tahir Imran,[a] You Gao,[a] Muhammad Azeem,[b] Muhammad Younis,[c] Jianan Wang,[a] Sanwan Liu,[a] Zhichun Yang,*[d] Zonghao Liu*[a] and Wei Chen*[a]

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Presently, perovskite solar cells (PSCs) have emerged as one of the most prominent photovoltaic (PV) technologies. However, the stability of PSCs is typically the primary challenge hindering their practical application. Among the various factors that affect PSC stability, potential-induced degradation (PID) is recognized as a significant reliability threat and can cause considerable damage to PSCs within a short timeframe. Accordingly, herein, we aim to review the progress on PID, its associated mechanisms, contributing environmental factors, and testing techniques by mainly focusing on various present PV technologies. Further, studies on PID are reviewed and valuable insights are offered for future research endeavors related to PID in PSCs and associated modules. Moreover, to enhance the commercialization aspects of PSCs, studies on the impact of structural and compositional characteristics, methodologies for the mitigation of environmental stressors, and the importance of interfacial engineering as future emerging trends are discussed.

Broader context

Climate change in recent years has increased the utilization of renewable energy resources. Photovoltaic (PV) technologies, one of the most important candidates as renewable energy resources, provide a real solution to lowering CO_2 emissions. Among the PV technologies, perovskite solar cells (PSCs) have emerged as the most promising component owing to their excellent power conversion efficiencies and cost-effective fabrication process. However, their stability is typically the biggest bottleneck in their mass production. Among the various other factors affecting the stability of PV technologies, potential-induced degradation (PID) is a reliability threat, which can cause considerable damage to them within a short timeframe. Thus, to speed up the commercialization of PSCs, the PID in PSCs needs to be addressed. Herein, we discussed its associated mechanisms, contributing environmental factors, and testing techniques by mainly focusing on various present PV technologies and summarized the reported literature on the PID in PSCs. Our contribution will provide a comprehensive summary and the latest insight into the PID in PSCs, leading to their eventual commercialization.

1. Introduction

Photovoltaics (PV) offers a clean energy source that is beneficial to reduce the environmental issues worldwide, particularly CO_2 emissions. Accordingly, its growth in the industry has become substantial over the last two decades, given that it is considered an economical, cost-effective, and sustainable technology. Renewable energy accounted for 29.9% of the global power generation till 2022, of which 70% was contributed by PV modules.[1] Recently, at the end of 2022, the highest delivery of 295 GW of PV modules was achieved, and the total installation capacity was recorded to be 258 GW, globally surpassing the total cumulative capacity of 1 TW.[2] The main factors responsible for the success of PV technology are its enhanced efficiency and stability along with low manufacturing cost, attracting interest from researchers in academia and industry. Following the increasing growth of the PV industry, academics, manufacturers, bankers, and investors have recently focused on the reliability of PV technology.[3,4] Reducing the manufacturing costs, boosting the power conversion efficiencies (PCEs), and extending the life span of PV systems are all crucial factors in enabling large-scale PV-based electricity generation. Although

[a] *Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China. E-mail: liuzonghao@hust.edu.cn, wnlochenwei@mail.hust.edu.cn*
[b] *Institute of Physics, Polish Academy of Sciences, aleja. Lotników 32/46, Warsaw 02-668, Poland*
[c] *Centre for Joining and Electronic Packaging, State Key Laboratory of Material Processing and Die & Mold Technology, School of Materials Science and Engineering, Huazhong University of Science and Technology (HUST), Wuhan 430074, China*
[d] *State Key Laboratory of Quantum Optics and Quantum Optics Devices, Institute of Laser Spectroscopy, Collaborative Innovation Centre of Extreme Optics, Shanxi University, Taiyuan 030006, China. E-mail: yangzhichun@sxu.edu.cn*

PV systems are considered dependable in the field, with minimal degradation and failure rates,[5–8] they are vulnerable to numerous significant failure mechanisms such as corrosion and delamination.[9–12] Recently, PID in PV modules has become significant among the evident reliability problems, since it has the potential to cause the catastrophic failure of PV modules in outdoor environments. Generally, module frames in grid-connected PV systems are grounded for safety, and solar panels are often connected in series to increase the voltage output. Consequently, a high voltage disparity is established between active solar modules and the grounded frame (Fig. 1a). Furthermore, PID occurs when a current, which is known as the leakage current, flows from active solar modules to module frames (or *vice versa*), depending on the polarity of the voltage. Thus, to provide an economical solution, industry is currently focusing on enhancing the voltage maximum of PV systems to 1500 V. However, with this achievement, the associated challenges, such as current leakages, also need to be addressed in the future.[13]

Crystalline silicon (c-Si) and amorphous silicon (a-Si) thin-film solar modules both experienced PID for the first time in 1985, according to the study by the Jet Propulsion Laboratory (JPL).[14,15] The Florida Solar Energy Center (FSEC), National Research Energy Laboratory (NREL), and British Petroleum (BP) Solar have studied several types of PV modules and their susceptibility to high voltage stress systems in the early 2000s.[16–18] Subsequently, in 2005,[19] it was investigated in an outdoor test array in Germany using SunPower's rear-junction n-type c-Si modules and Evergreen's standard modules using string ribbon-cast silicon wafers in 2008.[20,21] Numerous studies on the PID of conventional p-type c-Si PV modules have been conducted at institutions throughout the world since the term "PID" was proposed by Pingel *et al.* in 2010.[22–32] The reliability of several types of thin-film solar modules was also tested by

Hasan Raza

Hasan Raza received his Post-graduate degree in 2014 from Government College University, Faisalabad (Pakistan). He is currently a PhD student in the field of optical engineering in Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology (HUST), Wuhan, China. He is working on PID in perovskite solar cells and perovskite solar modules. His current research interests include optical devices based on inorganic/organic perovskites, especially perovskite solar cells.

Zhichun Yang

Zhichun Yang received his BS degree in 2014 from Yuncheng University, China, and his MS in 2017 and PhD in 2021 from Huazhong University of Science and Technology (HUST), China. He is currently an Associate Professor at the State Key Laboratory of Quantum Optics and Quantum Optics Devices, Shanxi University, China. His research mainly focuses on semiconductor optoelectronic devices, including perovskite solar cells and modules, photodetectors, and imagers.

Zonghao Liu

Zonghao Liu received his BS degree in 2011 and PhD in 2016 from Huazhong University of Science and Technology (HUST), China. He was a Visiting Student at the University of California, Los Angeles, USA, in 2015. From 2016 to 2017, he was a Research Assistant at Peking University, China. From 2017–2019, he worked as a Postdoctoral Scholar at Okinawa Institute of Science and Technology Graduate University in Japan. He is currently an Associate Professor in Wuhan National Laboratory for Optoelectronics of HUST. His current research focuses on optoelectronics devices based on inorganic/organic perovskites, especially perovskite solar cells.

Wei Chen

Wei Chen received his BS degree and PhD from the Department of Materials Science and Engineering, Tsinghua University. He worked as a Post-Doctoral Fellow with the Department of Chemistry, Hong Kong University of Science and Technology, from 2008 to 2010. He was a Visiting Scholar at the National Institute for Materials Science, Japan, from 2014 to 2015. He is currently a Professor at the Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology. His research interests cover the synthesis, understanding, and applications of functional nanomaterials and semiconductor thin films in next-generation solar cells, especially perovskite solar cells.

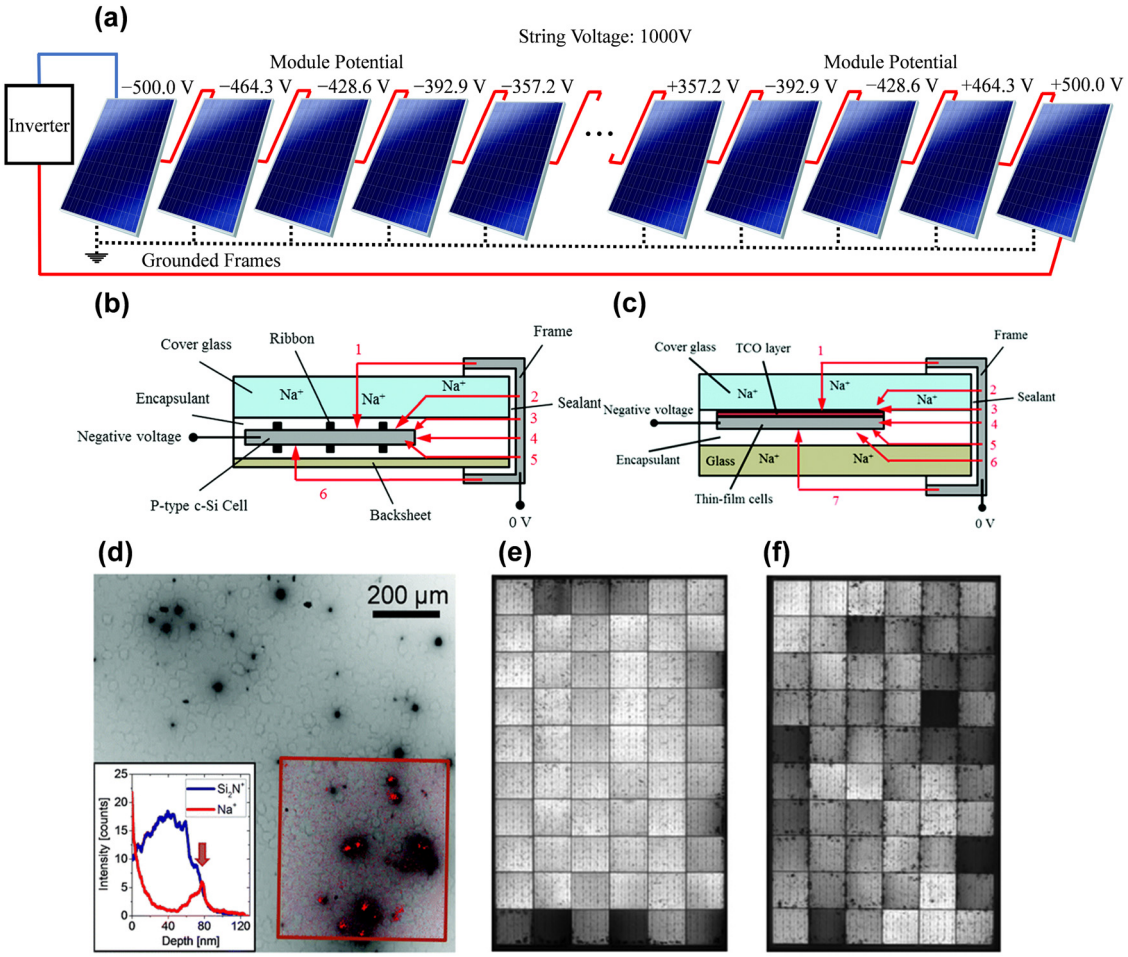

Fig. 1 (a) Solar module connection diagrams for the PV system. Since the module frames are grounded and interconnected in series, the bias voltage for each module grows as more modules are added to the circuit. Owing to the floating nature of solar cells and the high normal system voltage of 1000 V, both the first and last modules experience high voltages (−500 V and +500 V). (b) Conventional c-Si PV module cross-section and leakage current modeling for a glass encapsulant-cell with the encapsulant-back sheet package. When the module frame is grounded, the solar cells have a negative bias. The line with the arrowhead indicates the path of the leakage current. When the potential inside a cell is negative, positive ions, such as sodium ions (Na^+) from soda lime glass, (SLG) will drift in (*e.g.*, through path 1). (c) Demonstration of expected leakage current routes in a glass sheet back-covered thin-film PV module. A negative bias is applied to solar cells, with the module frame acting as the ground. The direction of the arrow indicates the flow of the leakage current. When the potential inside a cell is negative, positive ions such as Na^+ are attracted to it (*e.g.*, through paths 1 and 7). (d) At an acceleration voltage of 30 kV, an electron beam-induced current (EBIC) image of a section of a monocrystalline silicon solar cell with a large number of PID shunts. Na distribution at the SiN_x/Si interface, as determined by time-of-flight secondary ion mass spectrometry (ToF-SIMS), is displayed in the inset. (e) and (f) EL images of c-Si solar modules after a high-humidity, high-temperature climate chamber PID test (e) and with Al foil method after a PID test (f). The squares with dark shades depict the cell shunted by PID. Reproduced with permission.[61] Copyright 2017, the Royal Society of Chemistry.

exposing them to high-voltage stress in many studies.[33–37] The Solar Energy Research Institute of Singapore (SERIS) conducted reliability studies between 2009 and 2012 to ascertain the comparative sensitivities of different commercial absorber technologies towards PID. These studies employed a range of ten commercially available PV modules, including both thin-film and crystalline silicon (c-Si) modules.[35,37] Afterward, the PID of PSCs was firstly reported by Carolus *et al.* in 2019.[38]

However, although significant progress has been achieved in understanding PID in PV modules, many questions still need to be answered. Because of its complexity, researchers face significant challenges in addressing the PID phenomenon. The properties of the anti-reflective (AR) coating,[22,32] encapsulation materials, module design,[26,37] and system topologies are some of the numerous variables that affect the PID in PV devices or solar modules.[22,32] Various environmental stressors, including temperature, humidity, condensation,[26,27,39] wet or dry conditions of the glass surface,[27,40] and exposure to light, can lead to different degrees of power degradation. This degradation can occur even in the same type of modules.[41,42] Additionally, when the modules are exposed to the natural surroundings, the accumulation of soil on top of them may also influence their vulnerability to PID.[43]

The main contributions of the current review article are three-fold, as follows:

(i) Overview of the progress on PID in PV modules: a detailed overview on the progress in the field of PID in PV modules, focusing on PSCs and perovskite solar modules (PSMs) is provided herein. The existing research work is summarized and the advancements made in understanding and addressing the challenges associated with PID in PSCs highlighted. This contribution aims to consolidate the current state of knowledge and provide a comprehensive understanding of the PID phenomenon in PSCs.

(ii) Organization of existing knowledge: this review aims to organize the existing knowledge on PID in PSCs by extensively surveying and analyzing various literature sources. The information from diverse research papers, reports, and studies related to PID in PSCs and PSMs is collated. By structuring the information in a comprehensive and accessible manner, this review provides a valuable resource for researchers, industry professionals, and other stakeholders interested in PID mitigation strategies for PSCs. This contribution aids in combining the available knowledge and facilitating further research advancements.

(iii) Foundation for future advancements: another important contribution of this review is laying a foundation for future advancements in research related to PID in PSCs. By presenting the current progress, challenges, and potential solutions, we aim to inspire and guide further investigations in this field. Furthermore, the research gaps are identified and areas that require additional attention are highlighted, encouraging researchers to develop novel approaches and strategies to mitigate PID in PSCs. This contribution is beneficial to foster innovation and facilitate the commercialization of PSCs by addressing the hurdles associated with PID.

2. Leakage current and its pathways

The leakage current is a phenomenon that occurs in solar cells, where a small current flows across the cell even when it is not being illuminated by sunlight, which is often denoted as a ''dark current'' because it is generated by the intrinsic properties of the cell materials rather than the energy of incident photons. Various factors can contribute to the generation of a leakage current, such as impurities or defects in the functional layers and fluctuations in temperature. Higher temperatures increase the leakage current due to the availability of higher thermal energy to excite carriers inside PV devices. In a typical PV system (Fig. 1(a)), the presence of a significant voltage disparity between the grounded module frame and its active cells leads to the flow of current from the module frame to the individual solar cell. This phenomenon, also known as the leakage current, occurs due to the high electric potential differences existing between the module frame and the active circuit at each end of a module string. Consequently, the leakage current flows through the module packaging, which may significantly reduce the efficiency of the solar module. This leakage current is considered one of the reasons for the PID in PV devices or modules. Fig. 1(b) and (c) schematically show p-type c-Si and thin film-based solar modules, respectively, where the leakage current from the module frame to individual cells can flow through various pathways, as follows: (1) traveling along the surface of the front glass, penetrating the bulk of the front glass and encapsulant; (2) horizontally traversing through the bulk of the front glass and the encapsulant; (3) following the interface between the front glass and encapsulant, and then penetrating the bulk of the encapsulant; (4) directly passing through the bulk of the encapsulant; (5) moving along the interface between the back-sheet and encapsulant, and subsequently entering the bulk of the encapsulant; and (6) running along the surface of the back-sheet, and subsequently penetrating the bulk of the back-sheet and encapsulant.[22,32,40,44–46]

Current/voltage biasing is one of the significant factors in all types of solar modules. When electrically active solar cells are positively biased with respect to the module frame, as depicted in Fig. 1(b), the conventional direction of current becomes reversed. Due to the higher surface conductivity of the front glass in wet and humid circumstances, path 1 is frequently the most damaging way under outdoor operational environments.[40,47,48] The leakage current through path 6 is often neglected because the polymer back-sheet provides excellent resistance, and the metal back surface is used to offer full coverage. The front glass and the individual cell surface of thin-film solar modules are separated by a thin inner layer of transparent conductive oxide (TCO), as shown in Fig. 1(c).[49] In addition, the thin-film solar module typically has a glass sheet as a rear cover.[49] The leakage current paths in thin-film solar modules are comparable to that in traditional c-Si solar modules, despite the variations in module structure, with the exception of an additional path laterally through the glass at the rear of the module.[17,50–55] Furthermore, unlike the traditional p-type silicon solar modules, leakage current pathway 7 is not negligible.[53–55] PID can occur *via* both possible leakage current paths (1 and 7) due to the different PID sensitivity of each path. In the case of frameless thin-film solar modules, the leakage current may be reduced at the edges because of the excellent sealed edges and clamps. As a complex structure having various defects in the perovskite absorber layer, interfaces, or contact materials, PSCs may also experience leakage currents. Also, by applying a high voltage disparity during PID stress, a leakage current is also observed in PSCs.[38,56–60]

3. Factors contributing to the leakage current

PID is attributed to the leakage currents that arise from the voltage disparity between the ground and PV cells or modules. Therefore, any increase in potential difference or leakage currents between the grounded frame and solar cells or modules may eventually enhance the PID. The possible aspects affecting PID can be classified into the following three factors, *i.e.*, environmental, material,[26,27,39] and system or module design.[26,37] Humidity and temperature are the two primary ecological stressors that impact the leakage current in solar

modules. When the relative humidity is high, water vapor penetrates the surface of solar cells or modules, increasing their conductivity and leading to higher leakage current and larger PID. A similar effect may also be produced by an increase in temperature due to the increased mobilities of the ions in the active materials. The current for generating electricity can be weakened if there is an increase in the strength of the leakage current. However, although temperature and humidity can significantly impact PID, it is still challenging to be controlled.[26,27,39,47]

Generally, a PV system is comprised of a wide variety of components, and the susceptibility of the cell to PID can be determined, at least partially by the characteristics and attributes of each component. The AR coating, glass, and encapsulating materials are the major aspects responsible for the undesirable degradation.[22,32] Higher currents are attributed to the AR coating applied to solar cells, which enhances the amount of light absorbed by the cells. Alternatively, the AR coating has various effects on PID, depending on factors such as its thickness, refractive index, and coating homogeneity. Silicon nitride (SiN_x), a popular AR coating, can accelerate the PID process, while it accumulates some highly mobile sodium ions (Na^+).[62] Some glasses are more vulnerable to high leakage currents than others because they contain a significant amount of Na^+ ions and their mobilities increase when the devices are subjected to humidity or temperature stress, and the leakage current can penetrate the active layer. In this case, utilizing a type of glass with less Na, such as quartz instead of soda-lime glass (SLG), can potentially lower the susceptibility to PID.[24,39] The susceptibility to PID may also be affected by the permeability of the encapsulating material, while moisture has a direct effect on the conductivity of solar cells, modules and PV systems.[27,41] When the system potential becomes negative relative to the ground, the module usually starts to degrade as a result of PID. This problem can be easily fixed by performing functional earthing, in which the negative pole of the array is connected to the ground, and the system is forced to work only at a positive potential. This approach is the most effective, except for situations where the cell experiences electrocorrosion.[27,44] Recently, transformerless or non-isolated inverter technologies have been widely adopted, which do not allow the functional grounding of the array. Alternatively, another approach is the installation of a PV-offset box. During the night, this box applies a positive potential to the system, resulting in the discharge of particles and the reversal of the polarization effect.[19]

4. PID mechanisms

PID is commonly associated with multiple factors which are based on the specific type of PV technology employed. PID is likely to switch between modes when the same types of PV modules are subjected to varying environmental stresses. On a macroscopic scale, a thorough understanding of PID has been established; nevertheless, this concept is not yet completely understood on a microscopic scale. However, in the literature, several theories are utilized to explain the primary reasons behind the PID of PV technologies.

4.1. Shunting-type PID

PID-shunting, often referred to as PID-s, is predominantly observed in standard p-type c-Si solar modules. Several in-depth investigations revealed the main factors contributing to this type of PID in conventional p-type c-Si solar modules such as increased dark saturation current, decreased shunt resistance,[22,32,39,41,45,63–66] recombination of space charge area, and second diode term of ideality factor due to the recombination of non-linear shunting.[31,66,67] It is considered that Na plays a significant role in developing PID-s.[24,27] Specifically, Na^+ ions penetrate the Si crystals having defects by crossing the n^+–p junction under a negatively biased state from the SiN_x AR coating through the interface between Si and the AR coating. It is widely acknowledged that most of the module components, such as unpassivated edges or passivation layers, are considered to be responsible for the generation of Na^+ ions, which is the main reason for PID-s. The correlation between PID-s and Na^+ is supported by experimental results from scanning electron microscopy (SEM) with electron beam induced current (EBIC) measurements and dark lock-in thermography (DLIT), as shown in Fig. 1(d). These techniques have unveiled a strong correlation between the shunted areas of PID-affected solar cells and the accumulated of Na^+ ions at the interface between the Si substrate and the AR dielectric film.[28,29,68] This Na^+ contamination seems to originate from a single, easily identifiable source, and most studies have concluded that the SLG sheet is the source of Na^+ contamination. The presence of Na_2O in the SLG composition, ranging from 13% to 14%, leads to an increase in bulk resistivity at 25 °C, typically within the range of 10^{10} to 10^{11} Ω cm, due to the migration of Na^+ ions.[69] However, this Na^+ migration also contributes to the occurrence of shunting, resulting in a significant decrease in the efficiency of solar cells.[27–29,68,70,71] As the photocurrent decreases, the loss of carriers to the shunting paths becomes more pronounced. This leads to a decline in efficiency due to the increased severity of PID-s at low irradiance levels, which differs from the standard testing conditions. Evidence has shown that n-type passivated emitter rear totally diffused (PERT) cells, rear-emitter and interdigitated back contact (IBC) n-type c-Si cells, and silicon heterojunctions (SHJ) cells are also susceptible to this type of PID.[72] In the case of PSCs, some studies have shown the advantageous effects of incorporating Na-based salts in the absorber and transport layers or employing them as an interfacial layer.[73–79] Furthermore, the fabrication of PSCs involves the use of various materials in both the absorber and contact layers, mostly soft organic materials, which can easily migrate between the different layers of PSCs, providing shunting paths. Brecl *et al.* reported that the performance of their devices was affected due to shunt resistance and increased series resistance after performing a PID test.[57] Xu *et al.* also reported similar results for their perovskite/silicon tandem solar cell after PID testing,

where significant degradation occurred in the perovskite part of the cell.[58]

4.2. Polarization-type PID

Back in 2005, the polarization-type of PID was initially observed in n-type IBC solar modules. This phenomenon arises from the accumulation of charges.[19] Numerous n-type Si solar modules manufactured from PERT cells,[80–93] passivated emitter rear locally-diffused solar cells (PERL),[94] tunnel oxide passivated contact (TOPCon) cells,[95] and IBC cells,[19,96–98] including IBC cells with front-floating emitters, have shown to exhibit polarization-type PID.[36] All these cells usually require some dielectric passivation layer. Polarization-type PID has been reported predominantly in n-type c-Si cells, although it is not only limited to these specific cells.[98] It has been determined that charge accumulation on the front side of the AR coating or passivation layers is the main source of polarization-type PID. Swanson *et al.*[19] suggested that minority charge carriers were attracted to the interface between c-Si and the passivation layer by the charge accumulation resulting from the leakage current flowing across the module frame and cells. Consequently, minority carrier recombination at the interface is enhanced by the defect states at the interface. Compared to other PID types, polarization-type PID has a higher rate. Xu *et al.* confirmed that the 50% reduction in the efficiency of their perovskite/silicon tandem solar cell after PID testing was due to the accumulation of Na^+ ions. Akcaoğlu *et al.*[99] used the polarization type to study the PID in PSCs, dye-sensitized solar cells (DSSCs), and highly-efficient organic photovoltaic cells (OPVs).

4.3. Corrosion-type PID

A non-reversible PID found in different investigations[100–105] may occur on the rear side of bifacial passivated emitter and rear contact (PERC) solar cells due to the oxidation beneath the passivation layers, which leads to the increased recombination of charge carriers on the surface and reduced electrical and chemical passivation. Corrosion-type PID has been found in p-type c-Si solar modules and thin-film PV modules. According to the research conducted by Hacke *et al.*,[106] PID stress was found to cause the breakdown of metallization and the dissolution of SiN_x AR/passivation coatings. Furthermore, Sporleder *et al.* studied the corrosion-type of PID specifically on the back side of p-type bifacial PERC solar cells.[101–103,107] Generally, it is known that thin-film solar module degradation is attributed to the corrosion of TCO layers when subjected to a biasing voltage.[17,108–110] These results show that cathodic corrosion can damage solar cells when subjected to a negative biasing. Akcaoğlu *et al.*[99] studied the polarization and corrosion-type PID in PSCs, DSSCs, and OPVs.

5. Role of sodium ions in PID

When subjected to a negative bias, thin-film solar modules, including a-Si, cadmium telluride (CdTe), and copper indium gallium selenide (CIGS), have been observed to be susceptible to PID.[14,18,35,37,53,54,111–113] Na^+ migration is the primary instigator of PID in thin-film solar modules.[16,17,36,111,114,115] A strong electric field is generated between the shorted terminals of the cell and their frame when a high voltage is applied across them, which pushes the Na^+ from SLG into the active cells. There are two possible outcomes of this Na^+ penetration based on the absence or presence of moisture infiltration in the solar cell.

5.1. Absence of moisture

Under humid or dry conditions, where moisture has not yet penetrated the module, Na^+ is converted to elemental Na. This was observed as a darkening effect in both tin dioxide (Sn_2O) and zinc oxide (ZnO)-based TCO films.[114] It has been shown that the negative impacts of Na accumulation on electrical performance can be reversed by applying a reverse bias to solar cells or modules.[36,111] Also, the undesirable recombination occurs in semiconductors when the junctions have too many impurities. Yamaguchi *et al.* found that the open circuit voltage (V_{OC}) and fill factor (FF) of CIGS solar modules with a ZnO-based TCO layer were reduced by more than 40% and 50%, respectively, with only minor changes to the short-circuit current (I_{SC}), shunt resistance (R_{sh}), and series resistance (R_s).[111] Moreover, it was demonstrated that the diode ideality factor (n) or the density of recombination centers, according to the one-diode model, escalated from 1.4 to approximately 9.0 within a span of two weeks for the cell affected by PID.[111] Consequently, their research showed that increased recombination is primarily responsible for the PID of CIGS solar modules.[111]

On the contrary, the presence of Na accumulation in thin-film solar modules can lead to various forms of PID. Fjällström *et al.* conducted experiments, which revealed a degradation in the V_{OC}, J_{SC}, and FF values of a CIGS solar module over time.[36] The different sites of Na^+ accumulation in Yamaguchi *et al.* and Fjällström *et al.* studies may be due to the differences in their experimental arrangements. Yamaguchi *et al.* conducted an experiment, where they injected Na from the light-facing side of the glass. They observed that the damaged sample exhibited a higher Na signal intensity in the ZnO layer compared to the control sample. The differences in the sites of Na^+ accumulation observed in the studies by Yamaguchi *et al.* and Fjällström *et al.* may be attributed to variations in their experimental setups. Yamaguchi *et al.* injected Na from the side facing the light, observing a higher Na signal intensity in the ZnO layer of the damaged sample compared to the control sample.[111] In the study by Fjällström *et al.*, Na was introduced from the rear side, resulting in increase in Na content in both the upper region of the CIGS and the cadmium sulfide layer.[36] Both studies concluded that the Na accumulation is the primary cause of the PID, and degradation can be recovered by applying the reversed biased voltage. Furthermore, Hacke *et al.* found that CdTe solar modules exhibited a shunting mechanism accompanied by an increase in series resistance.[116] In their study, they observed a reduced degradation under low humidity, while accelerated

degradation at 85 °C under 85% relative humidity (RH) under PID stress. However, despite these findings, there is still insufficient research on the origins of PID processes in thin-film solar modules.

5.2. Presence of moisture

Researchers found a different PID mechanism in many studies when moisture enters the modules, especially under humid conditions.[16,17,42,51,114,117,118] In addition to the surrounding environment, the packaging quality of the module can affect how much moisture gets inside. For example, a module with high-quality packaging will be protected from moisture damage even in wet environments. However, Na^+ ions and moisture ingress together will cause irreversible electrochemical degradation of the tin oxide (SnO_2)-based TCO coating.[16,17,61,114,119–121]

Consequently, the adhesion between TCO and the substrate is disrupted. Na serves as a reactant and its accumulation intensifies the mechanical stress at the respective interface.[114] When this mechanical stress is too high, cracking and, eventually, delamination of the TCO film is initiated.[16,17,114] There is another possibility in which fluorinated TCO compounds, such as SnO_2:F, can potentially operate through a distinct mechanism due to the interaction of fluorine with water, leading to the formation of hydrofluoric acid at the interface.[114] Consequently, this acid formation may rupture the bonds between tin and oxygen. ZnO is significantly less susceptible to chemical attack by atomic hydrogen compared to the SnO_2-based TCO layer.[122] Accordingly, the thin-film solar modules that utilized a ZnO-based TCO layer did not exhibit any noticeable delamination effects.[16,114]

5.3. Effect of Na incorporation in PSCs

Recently, numerous studies have incorporated Na-based salts in the absorber and transport layers or as an interfacial layer in PSCs to improve their performance under specific conditions.[73–79] Dong *et al.*[78] and Li *et al.*[77] used an electron transport layer (ETL) doped with sodium chloride (NaCl), while Lin at el.[79] physically blended it in the ETL and observed the diffusion of Na^+ from the ETL to the perovskite layer, resulting in an enhanced perovskite grain size and passivation of the grain boundaries, improving the charge transport and device performance. However, the enhancement in performance cannot be primarily attributed to the Na^+ ions because Cl^- may have the same effects as that found in several other studies.[123–127] Lee *et al.*[73] added NaCl as an additive in the precursor solution of perovskite and achieved a 48% improvement in PCE. Di *et al.* introduced an ultrathin layer of NaCl between the nickel oxide (NiO_x) and the perovskite layer and improved the V_{OC} of the solar cell. Chen *et al.*[75] and Dagar *et al.*[76] used different alkali salt (including Na)-based interfacial layers to improve the stability and efficiency of the PSCs. In contrast to PID, in which Na^+ ions enter solar cells through the SLG, all these studies discussed the beneficial effects of the incorporation of Na as a dopant in different layers of PSCs or as an interfacial layer between layers.

However, Kosasih *et al.*[128] were the first to investigate the diffusion of Na^+ ions from SLG along the P1 lines during the device fabrication process and its impacts on the performance of n–i–p and p–i–n PSMs. They found that the charge transport layer and perovskite film annealing process supplied sufficient energy for Na^+ to diffuse vertically in the P1 lines and laterally into the active area with a vertical depth up to 360 μm (Fig. 2). They observed that the annealing process during the fabrication of the charge transport layer was the main reason for this diffusion, given that they used different temperatures for different times. Na–Br was formed when Na^+ diffuses into a perovskite film containing Br, leading to Br-poor, and I-rich perovskite in the region of the P1 lines. Na–Br passivated defects in the perovskite layer, which reduced the non-radiative recombination, improved the perovskite luminescence by a factor of up to five, and increased V_{OC}. Moreover, studies on doping Na^+ deliberately in the perovskite layer revealed a decrease in the power output of the module.[74,129,130] They concluded that there was a chance of continuous Na^+ diffusion throughout the lifespan of a module, particularly when it is accelerated due to an electric field (as in the case of PID) and increased temperatures achievable under actual field operation.

6. PID testing methods for PV technologies

To guarantee a 20- to 25-year lifetime in the PV field, solar panels, the most reliable part of PV solar systems, are typically tested indoors under severe conditions. Various indoor test methods have been developed to determine the PID-vulnerability of solar modules by combining different stressing variables. These test techniques determine the module damage, and sometimes, even identical modules subjected to similar PID test conditions may have diverse power losses. Also, there is a lack of clarity regarding the correlation between the PID testing methods performed in labs and outside. Furthermore, it is necessary to learn about the various PID test methodologies to design a standard PID qualification test that can assess the PID stability of solar modules. Herein, we discuss the ongoing PID laboratory test methods utilized at the module and cell level, together with their advantages, disadvantages, and applications.

6.1. Testing methods of PID at the module level

Different testing methodologies of PID at the module level are being used in outdoor and indoor testing, depending on the parameters of the module. PID testing methods also provide diagnostic studies and understanding to discover the origin of PID.

6.1.1. Climate chamber method. The climate chamber method involves subjecting PV solar modules to extreme temperatures and humidity under high voltage for PID testing.[26,27,42] It is performed by putting the modules inside a climate control chamber. In this method, the grounded frame

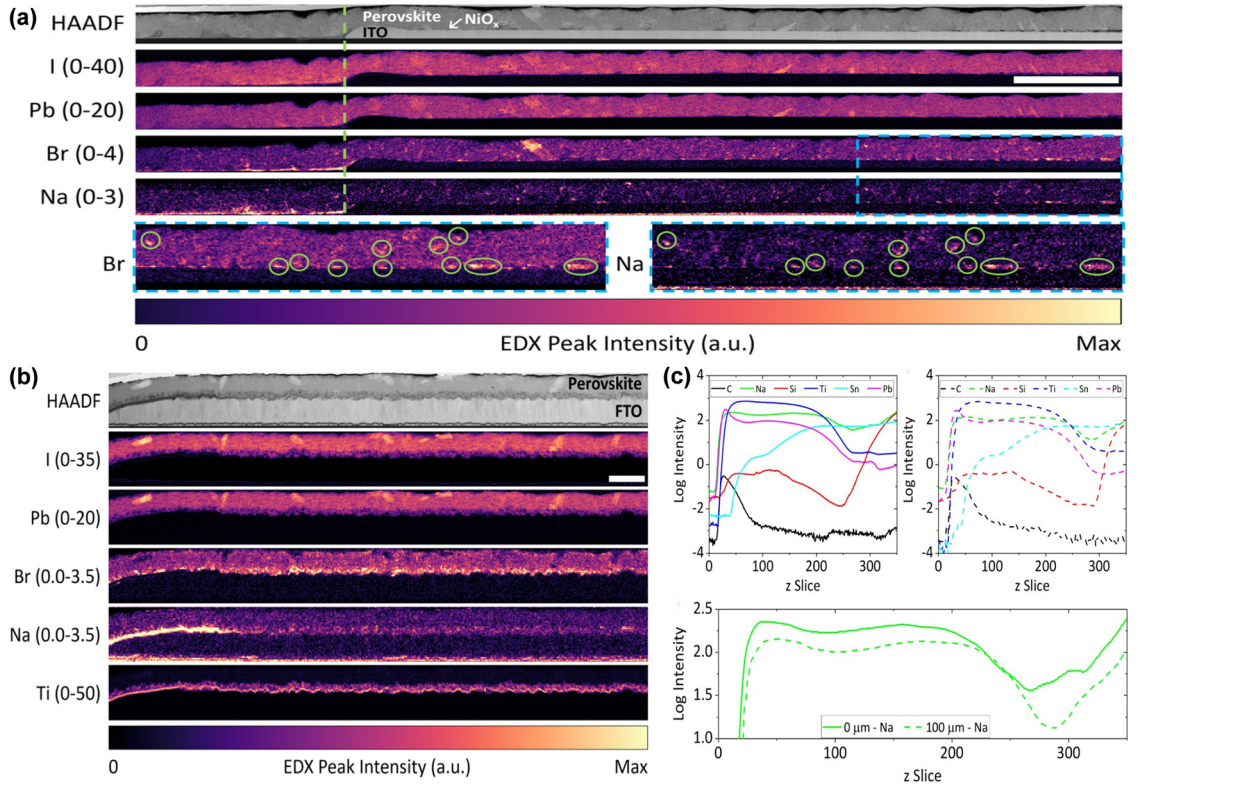

Fig. 2 (a) Scanning transmission electron microscopy-high angle annular dark-field imaging (STEM-HAADF) cross-sectional images and scanning transmission electron microscopy-energy dispersive X-ray (STEM-EDX) peak intensity maps of the NiO_x-based device. The dashed green line shows the P1 line edge. Green circles in the bottom row indicate the Na–Br correlation. The range of the colour scale used for each map is indicated by the numbers in brackets, where the scale bar represents 2 μm. (b) Device STEM-HAADF cross-sectional images and STEM-EDX peak intensity maps of TiO_2. (c) Nanoscale secondary ion mass spectrometry (NanoSIMS) elemental depth profiles collected from 0 μm and 100 μm away from the P1 line in the TiO_2 device, where higher slice numbers are closer to the glass substrate. A zoomed-in comparison of the solar panel Na depth profile shows a lower Na signal intensity further away from the P1 line. Reproduced with permission.[128] Copyright 2022, Wiley-VCH.

is connected to the positive terminal, whereas the short-circuited leads of the modules are connected to the negative terminal of a source having a high voltage, as represented in Fig. 3b. This is the most commonly employed configuration for this test setup. Furthermore, particular types of equipment can be used to monitor the leakage current and evaluate the functionality of the module at high voltage and temperature stress without taking it out of the flashing chamber. In this case, Spataru *et al.*[131] developed a superposition-based[132] *in situ* dark current–voltage characterization method. The primary test standard, IEC 62804-1,[133] follows a similar procedure in which modules are subjected to stress in a climate chamber for 96 hours. During this period, the modules are exposed to conditions of at least 60 °C temperature and 85% RH. Additionally, an applied voltage equivalent to the maximum rated system voltage of the module is applied. Instead of establishing strict pass/fail criteria, these tests are designed to provide repeatability in results from different laboratories. PID effects can also be studied by using alternative temperature, humidity, and voltage combinations such as 85 °C, 85% RH, and 1000 V, respectively, as proposed in the IEC 62804-1 standards.[133]

Given that humidity and temperature immensely impact the PID effects, careful monitoring of the chamber conditions is required during a PID test to ensure repeatability. Two PID-affected modules were examined by Koentopp *et al.* in a chamber with a controlled environment and stable humidity, and two extra samples were analyzed in a chamber with considerable humidity variations.[41] Based on these experiments, they discovered that a significant change in humidity induced additional stress in the modules.[41] This is most likely the result of condensation or moisture build-up on the upper side glass of the module. Additionally, the adjustment of the ramping process could help to prevent this condensation.[41] However, increasing the chamber temperature will always lead to a difference between the chamber and the module temperatures. A significant temperature difference exists between the chamber ambience and the module, and the ramping is excessively rapid. This can result in condensation accumulating on the upper side glass of the module, which impacts the reliability of the test. Thus, it is necessary to optimize the ramping rate for humidity and temperature to prevent condensation and minimize the ramping time. Moreover, the module temperature must be stabilized before the humidity is adjusted to the required stress level, and the humidity must be stabilized again before the voltage bias is applied according to IEC 62804-1.[133]

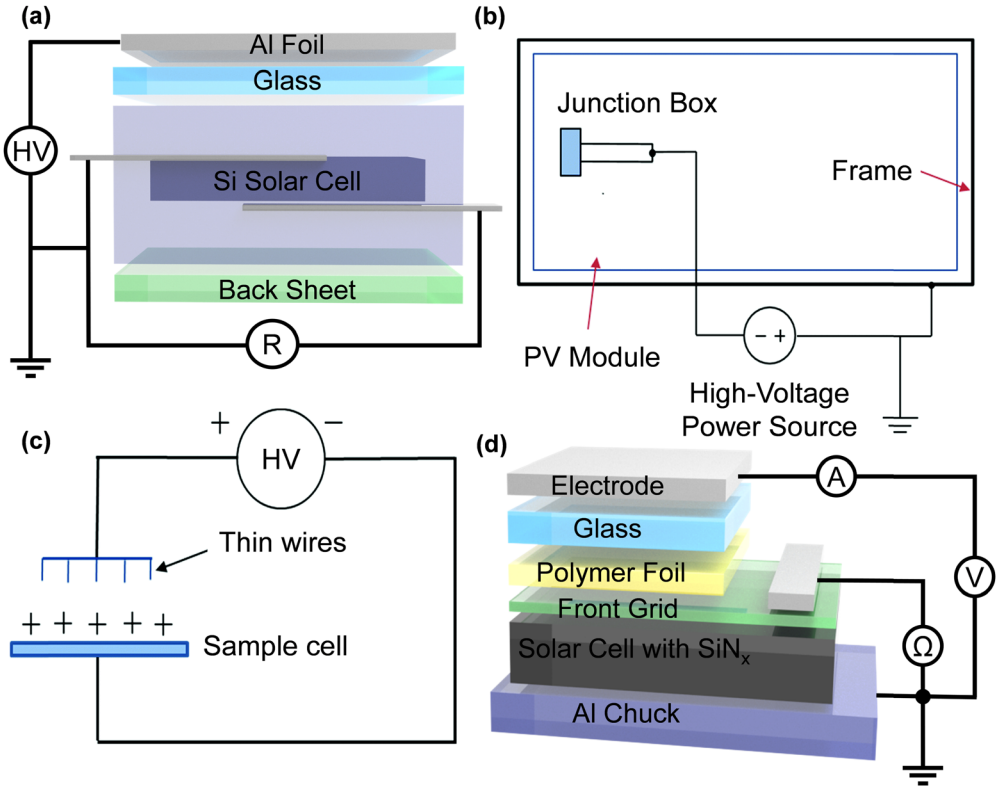

Fig. 3 (a) Schematic representative diagram of the Al foil method for an Si solar cell. (b) Schematic representation of PID test arrangement in a climate chamber. The two wires of PV solar modules are joined and connected to the high-voltage negative terminal, while the module frames are grounded. (c) Schematic illustration of PID testing corona-discharge assembly. The high-voltage power supply is denoted by "HV". (d) Schematic representation of the module-like layer stacks testing method developed by Fraunhofer CSP. Reproduced with permission.[61] Copyright 2017, the Royal Society of Chemistry.

6.1.2. Al or Cu foil method. In the Al or Cu foil method, a conductive layer of Al or Cu is used on the upper side of the front glass of the module, differentiating it from the climate chamber test method.[27] This test has also been introduced in IEC 62804-1 as an alternative to the climate chamber method of PID testing, with the only difference of additional Al or Cu foil. The Al or Cu foil creates a conduction path on the glass surface, providing the same effects as that of the higher humidity conditions. A precise temperature adjustment is required in this experimental arrangement, while the Al foil reduces the need for humidity adjustment. In addition, the Al foil needs to be pressed firmly on the glass surface, such as with the help of a rubber mat, causing the contact to be uniform.[42] One of the advantages of the Al or Cu foil PID test over the chamber PID test is that it requires less humidity control and can measure significantly higher degradation rates at the same applied temperature. Unlike Al foil PID tests, chamber PID tests include aspects of the natural environment (such as increased temperature and humidity) and can distinguish PID solutions (such as fully electrically separated module mounts).[42,134,135] Consequently, the climate test chamber is generally more related to the field than the Al foil method.

For modules with polymeric back-sheets, extended exposure to higher temperature and humidity in a chamber (*e.g.*, 85 °C/85% RH) may cause other PID processes, such as thinning of the SiN_x layers[24,31,136] observed in the field.[137] PID effects often begin at the frame,[134,135,138] as exhibited in the electroluminescence (EL) results of PID-stressed modules in the field, and also confirmed by the findings of the chamber PID test (Fig. 1(e)).[71,134,135,137] When using the Al foil method, the frequently observed degradation pattern is different because the PID-affected cells are not evenly distributed (Fig. 1(e) and (f)).[71,134,135,139] However, some reports in the field represent that these degradation patterns are similar to that observed in the Al foil PID test.[134,140] The increased surface conductivity of the glass may be due to the electrical behavior of the AR coating or the conductive soiling of the glass.[43,141] High resistivity in the encapsulating material is another explanation for the inconsistent findings.[141]

Pingel *et al.* employed finite element modeling to investigate the impact of the bulk resistivity of the encapsulating material on the local electrical potential distribution across the surface of the module.[141] As the bulk resistivity of the encapsulating material decreases, there is an increase in the potential difference between various sections of the module surface. When the encapsulation material possesses a high bulk resistivity, comparable to the conduction in a water film or Al foil characterized by significantly greater PID resistance, the potential across the surface of the module is uniformly distributed. Using a glass with high resistivity yields the same result as using a

highly resistant encapsulant.[46] All the studies reported to date on the PID of PSCs used the Al foil method.

6.2. Testing methods of PID at cell level

Investigating PID testing at the cell level is also beneficial given that it presents an opportunity to gain insights into the fundamental underlying mechanisms of this phenomenon. It is quite challenging to isolate a PID-affected encapsulated cell for microscopic investigations. Moreover, single solar cells can be evaluated without investing in the more expensive process of fabricating modules.

6.2.1. Corona discharge assembly method. Understanding the underlying mechanisms of PID demands a detailed analysis of this phenomenon at the microscopic level. However, the techniques used to study PID in modules are not suitable for cells because they can rapidly harm them. Thus, to generate PID in solar cell samples, the corona discharge assembly method was utilized,[39,45,63,142] and a schematic of the corresponding test setup is shown in Fig. 3(c). Technically, positive ions are deposited on the front side of the sample, which are generated by applying a high potential to the tip of a thin wire. Subsequently, these positive ions spread throughout the sample cell, inducing an electric field; however, the nature of these ions is not the same as that of ions deposited during the Na^+ ion migration in modules under the operational process. Na^+ is believed to be already present on the cell surface and varies in concentration, creating PID in this testing method.[62,143] There is a constant possibility that the ions produced by the corona discharge may potentially damage and modify the characteristics of the SiN_x film, thereby diminishing the effectiveness of this approach. Furthermore, this procedure fails to account for the significant influence of the encapsulating material and the glass sheet on the distribution of the electric field, which is a notable limitation.

6.2.2. Module-like layer stack method. Performing PID testing at the cell level using a corona discharge assembly offers several advantages but also presents notable drawbacks. In this case, some of its flaws can be mitigated by using a new PID test approach that simulates a laminated module and considers the effects of the packaging materials.[67,71] The Fraunhofer Centre for Silicon Photovoltaics (CSP) developed a PID testing methodology for c-Si-based PV technologies to replicate the module-like structure (Fig. 3d).[67] To ensure a uniform temperature throughout the solar cell, it is positioned on an Al chuck, allowing temperature regulation as needed.[67] The solar cell has an encapsulant foil covering its exposed front surface, followed by a transparent glass sheet.[67] By applying a high voltage between the Al chuck and the metal block, establishing the desired potential difference across the stacked layers can be achieved.[67] This configuration allows for PID testing on samples without the need for lamination. Moreover, it enables the detachment of the affected solar cells from the encapsulating layer and glass sheet without any contamination, facilitating a comprehensive examination of the underlying PID mechanisms.[67] Additionally, by introducing a small reverse bias voltage between the solar cell front and back contacts, its shunt resistance can be measured *in situ*. In this way, the development of PID in the sample cell can be tracked in a quasi-continuous manner.[67]

7. PID in thin film solar cells/modules

Thin film solar cells (TFSCs) utilize thin layers or combinations of thin layers composed of various semiconductive materials as the absorber layer.[144] The highest recorded efficiencies for different thin-film PV technologies are currently 23.3% for CIGS (concentrator), 23.6% for CIGS, 22.4% for CdTe, and 14.0% for amorphous Si:H (stabilized).[145] Unlike silicon solar modules, thin-film solar modules are usually fabricated by connecting the isolated adjacent subcells in series to form a module. Thus, the voltage of thin-film solar modules is much higher. Together with manufacturing cost and module efficiency, the levelized cost of electricity (LCOE) is influenced by the probability of failures and the efficiency degradation over time. Thus, PID is also crucial for TFSC technologies as the system voltages reach 1000–1500 V in the field and the extremely large potential difference between the cells and the frame may degrade the module and cause power production losses. The NREL identified a number of stressors that caused TCO delamination and electrochemical corrosion-based damage to a-Si and CdTe modules, such as moisture ingress, mounting configuration, and conductivity caused by humidity on the module surfaces, which affected the leakage current to the ground.[17] Cell-isolating laser scribe lines that fully pierce the front glass surface, including the thin diffusion barrier, have been linked to shunting. This occurs when Na^+ is forced into the isolated region in negative strings.[146] In this specific mechanism, it was observed that the shunting could be reversed by changing the polarity of the voltage to positive bias. Under similar testing conditions, it has been found that CIGS PV systems exhibit greater resistance to PID compared to multi-crystalline Si and a-Si.[115] CIGS modules with the standard size have also demonstrated degradation in PID tests and exhibited the ability to reverse the degradation. However, PID will only occur if the potential differences are sufficiently significant, which is highly probable given the desire to increase the maximum system voltages to 1500 V and potentially even higher in PV power plants. Thus, to mitigate this potential for unreliability, it is crucial to comprehend the mechanisms that lead to degradation and accurately measure and predict their impact.

The testing methodologies used to detect PID may vary across thin-film and crystalline silicon technologies because of their different sensitivities to environmental stress factors and the mechanisms by which these factors affect them. In particular, the TCO corrosion in thin-film modules, which is indicated by system voltage stress, is thought to happen due to the ingress of moisture, and it is not easily reversible.[147] Nevertheless, the degradation of the p–n junction in traditional silicon modules does not always depend on moisture ingress and can be reversed significantly.[32] Contrary to traditional crystalline silicon module technology, research has

demonstrated that there can be a connection between the level of power degradation observed in the accelerated testing of thin-film modules and the degradation observed in field-mounted modules, which can be attributed to Coulombic correlations.[55] Due to these correlations, predicting the increase in leakage current in different outdoor settings should be feasible by analyzing the amount of Coulombs transferred in connection to weather conditions. This approach has been suggested to quantify PID in real-world scenarios.[148] Nevertheless, thin-film modules may experience various degradation mechanisms due to system voltage stress. The correlation between Coulombs transferred from the module cell circuit to the ground and the degradation of the module power caused by system voltage stress may have limitations. It is feasible for this correlation to exist for specific mechanisms but not for others.

The application of voltage to p-type silicon solar cells causes the infiltration of Na ions in the stacking faults, which then function as shunt pathways, leading to degradation.[29,68,70,149] Conversely, the accumulation of positive charges on the surface leads to the recombination of electrons near the emitter, ultimately leading to the degradation of n-type solar cells.[86,150] Charges from glass may mediate the leakage current in both cases. The efficiency of CIGS thin-film solar cells can be improved during fabrication by injecting a specific amount of Na, given that the Na content of CIGS has an impact on the properties of solar cells.[151–154] Lechner *et al.* demonstrated the correlation between charge accumulation and degradation under negative bias in their study on CIGS thin-film modules in the field.[55] Boulhidja,[155] Hacke,[156] and Liu *et al.*[157] also found that high negative voltage affects the CIGS PV module performance. Akurai *et al.* showed that a negative bias did not influence their chalcopyrite-based $Cu(In,Ga)(S,Se)_2$ modules in the field. Instead, they observed that a positive bias significantly impacted the maximum power increase (within $\pm 2\%$).[158] Muzillo *et al.*[159] reported two PID mechanisms. A high potential (1000 V) to the front glass causes alkali metal cations to collect in the i-ZnO buffer, increasing the shunt conductance and slowly reducing the FF. Alternatively, p–n junction PID is driven by applying a high potential (1000 V) to the back glass, which rapidly decreases the carrier concentration due to the accumulation of alkali metal cations, particularly Na^+ ions, near the junction, where they compensate with the majority carriers to reduce the built-in field and V_{OC}. To lower the FF, the cations may operate as junction shunt routes. Yilmaz *et al.*[160,161] solved the gap between laboratory-made CIGS in-depth microanalyses without encapsulants and front glass sheets that show Na accumulation in CIGS layers and field modules with glass sheets and encapsulants that only measure the current–voltage and leakage current. Na was absent in the ZnO layer, indicating Na migration from the substrate glass to the solar cell. The electrical properties of the absorber layer declined with Na accumulation. Other authors also explored the influence of introducing a voltage between the front glass of CIGS modules and the cells.[53,111,162] According to Alonso-Garcia, the impact of PID on the front glass may be considerably less than on the rear.[163] Thus, it appears that the primary degradation mechanism is p–n junction PID, as explained by Muzillo *et al.*,[159] which is activated by applying a high potential to the back glass. Yilmaz *et al.*[164] suggested a system-level inverter structure grounding the negative end of strings to avoid PID in thin film solar modules, especially in CIGS, and modifying the mounting system and frame to reduce leakage currents, but this probably would not prevent morning dew from causing leakage current peaks. Encapsulants possessing high electrical resistivity or glasses with a lower Na concentration can be employed at the module level. Fjällström *et al.*[36] showed that cells on glass without Na did not experience any form of degradation. The alkali-free glass exhibited remarkable insulating characteristics, effectively inhibiting any charge transfer. Muzzillo *et al.*[113] reported similar findings using less-conductive potassium-rich borosilicate glass (BSG) substrates, which reduced the leakage current by 35-fold under high voltage. They discovered that the SLG and BSG substrates degraded similarly after adding equal amounts of cations.

At the cell level, Salomon *et al.*[165] employed the addition of a barrier layer or denser molybdenum (Mo) back contact to improve the stability against PID. They found that the PID-resistant cells maintained their stability despite the large amount of charge travelling through the glass substrate. Using the same strategy, Muzillo *et al.*[166] showed CIGS devices with up to five times the failure time of their standard devices. Their modified devices had an extra layer of Al_2O_3 placed between the SLG and the Mo back contact. Importantly, the leakage currents observed in the reference and Al_2O_3-coated samples were comparable. By adding a barrier or Mo with lower porosity, as reported by Salomon *et al.*,[167] the samples were more than 10-times more stable against PID.

Compared to other PV technologies, CIGS PVs have higher resistivity to PID, with only a small number of solar modules impacted by this voltage stress. The present aim of building PV power plants with higher system voltages may increase the chances of the CIGS system having PID failures. Hence, it is crucial to analyze and comprehend the underlying factors responsible for this degradation phenomenon. In PID evolution, the leakage currents and Na migration from the glass to the solar cell stack are related. Numerous field investigations found a strong correlation between total transferred charge and PV module power degradation, as measured by the leakage current. This finding opens the door to the possibility of estimating the module lifetime through simulations based on the direct linkage between accelerated laboratory testing and field measurements. However, microscale laboratory research primarily focused on examining the significant influence of Na in the development of PID. Different observations of Na migration have led to varying opinions about the degradation mechanisms. Na migration from the substrate glass to the CIGS/CdS contact can damage the p–n junction and the cover glass, resulting in the corrosion of the TCO layer. These degradation mechanisms were reflected in electrical performances with a decline in V_{OC} and FF with a steady I_{SC} (but in severe situations), and shunting and overall poor *I–V* characteristics were also recorded. The electrical performance reflected

the degradation mechanisms by causing a decrease in V_{OC} and FF, whereas I_{SC} remained relatively stable (unless in severe cases). Additionally, shunting and overall poor *I–V* characteristics were also observed. At the system level, it is essential to have an electrical layout that includes a carefully designed grounding system and limited peak voltages. At the module and cell level, the resistance to PID can be enhanced by minimizing both the leakage current and Na migration. Encapsulants and glass with high electrical resistance are recommended. The cover and substrate glass should be low-sodium. The incorporation of a Na diffusion barrier layer proved to be beneficial at the cell level. Furthermore, the PID in CIGS PV systems can be reversible and modules may regain their initial electrical properties through dark storage, light soaking, and biasing in reversed polarity. Moreover, PSCs are also classified as thin film-based solar cells. Therefore, studying the phenomenon of PID in TFSCs may provide valuable insights into the mechanisms and processes for mitigating it in PSCs.

8. PID in perovskite solar cells

Over the past decade, PSCs have undergone remarkable advancements, surpassing the efficiency of well-established thin-film PV technologies such as CIGS and CdTe,[145,168] and these developments have positioned them as highly efficient thin-film PV devices.[169–171] Currently, the highest recorded efficiencies for single-junction perovskite and tandem perovskite/silicon solar cells are 26.1% and 33.7%, respectively.[145,172–174] Scalability improvements by coating large-area perovskite films have made it possible to fabricate solar modules, and eventually, perovskite-based panels and systems have entered the market, raising the significance of module stability requirements.[175,176] The primary source of doubt concerning the reliability of PSCs is the sensitivity of the perovskite absorber towards light, temperature, electrical field, oxygen, and humidity as well as the undesirable ion migration.[6,177–181] Thus, long-term reliability has received much attention, mainly in the laboratory with controlled temperatures and lighting conditions and in natural outdoor situations.[182–184] Furthermore, recent results have shown a remarkable enhancement in stability for several thousand hours.[185–188] PSCs must show commercial viability in the PV field by demonstrating a long, sustainable lifetime, high efficiency, and low cost.[182,189]

To successfully commercialize PSCs, it is inevitable to address external stress factors such as light, heat, moisture, oxygen, and electric field that arise during real-world device operation. Remarkably, PID has now been recognized as a prominent risk across various established commercial technologies, given that it can cause substantial performance degradation within a relatively short timeframe.[61,190] Compared to commercialized PV technologies, PSCs are currently at a point of development where standardized test protocols should be established on account of their unique operational stability characteristics. In contrast, it is imperative to address and understand the effects of PID on the operational stability of perovskite modules during the early stages of commercial development. This proactive approach will contribute to the long-term durability and lifespan of the modules.[191] The existing studies on PID in PSCs and perovskite/silicon tandem solar cells (TSCs) are summarized in Table 1.

8.1. PSCs are not PID resistant

The first study on PID in PSCs was performed by Carolus *et al.* in 2019,[38] and their results showed up to 95% performance loss under 18 h of PID stress of 1000 V. They used an encapsulated n–i–p-structured device, which consisted of an SLG substrate, indium tin oxide (ITO) front contact, SnO_2 ETL, perovskite layer as the absorber, 2,2′,7,7′-tetrakis(*N*,*N*-di-4-methoxyphenylamino)-9,9′-spirobifluorene (spiro-OMeTAD) as the hole transport layer (HTL), and a gold (Au) back contact. The Al foil method has been used to study PID in the devices, as mentioned in IEC62804-1, while the solar cells were placed in an environmental chamber at 60 °C and 60% RH. As illustrated in Fig. 4(a), the PID-testing setup used in this experiment consisted of an encapsulated cell using the Al foil method with an applied electric field. The device behavior under thermal stress has been investigated using the same encapsulated reference cell, as in previous PID investigations of other PV technologies, which revealed that an increase in temperature can accelerate the PID process.[61,68,111] Both the reference and PID samples were subjected the same external thermal environment, except a high voltage was applied across the PID sample. Because the spiro-OMeTAD HTL, covered by an Au film, is sensitive to temperature, increasing the temperature during the PID experiment caused the efficiency to drop even further.[192]

Carolus *et al.* conducted *J–V* measurements of the reference and the PID sample under the standard test conditions to verify the effects of PID stress on the performance of PSCs.[38] After thermal exposure for 18 h, they found that the P_{max} of the standard device dropped by 26%, owing to the 18% drop in FF, 6% drop in short circuit current density (J_{SC}), and 4% drop in open circuit voltage (V_{OC}), whereas after 90 h, the P_{max} of the PID sample dropped by 42%, owing to the 24% drop in FF, 14% drop in J_{SC}, and 11% drop in V_{OC} (Fig. 4(b)). In addition, the *J–V* curves of the PID sample both before and after stress implementation and recovery were included. Temperature-induced morphological deformation of the spiro-OMeTAD HTL capped by an Au rear contact is a well-documented source of this degradation.[192] A much higher degradation rate was observed in the PSCs compared to the control sample, making it evident that the used material was susceptible to PID. Under the abovementioned conditions, a 95% decrease in P_{max} was observed after 18 h of PID stress, mainly due to the 94% decrease in J_{SC} and 14% in FF, but the V_{OC} remained almost unchanged (increased by 4%). They hypothesized that the potential difference of 1000 V may induce large diffusive fluxes of Na^+ in their case, as also observed in other PID studies.[32,36] The efficiency of the device may decrease due to the oversaturated perovskite layer with mobile species, given that it can alter the bulk properties of the perovskite film[193] and block

Table 1 Summary of studies on PID on PSCs and perovskite/silicon tandem solar cells

Year	Device structure	Perovskite composition	Active area (cm^2)	PID testing time (h)	Applied potentia (V)	Biasing	Conditions	Recovery (h)	Ref.
2019	n–i–p	$Cs_{0.1}FA_{0.9}PbI_{2.775}Br_{0.225}$	2 × 0.5	18	1000	—	60 °C, <60% RH	72	38
2021	n–i–p, p–i–n	$Cs_{0.1}FA_{0.9}PbI_{2.865}Br_{0.135}$	1	18	1000	—	60 °C, <60% RH	—	56
		$Cs_{0.18}FA_{0.82}PbI_{2.82}Br_{0.18}$							
2021	p–i–n	$Cs_{0.05}(FA_{0.83}MA_{0.17})Pb_{1.1}(I_{0.83}Br_{0.17})_3$	1	168	±500, ± 1000	Negative	25 °C, 20% RH	—	57
2022	Perovskite/silicon tandem	Double-cation perovskite	1	24	±1000	Negative	60 °C, 20% RH	24	58
2023	p–i–n	$Cs_{0.05}(MA_{0.15}FA_{0.85})_{0.95}Pb(I_{0.85}Br_{0.15})_3$	1.2	55	±1000	Negative	25 °C, 20% RH 60 °C, 60% RH	90	59
2023	p–i–n	$Cs_{0.05}(MA_{0.15}FA_{0.85})_{0.95}Pb(I_{0.85}Br_{0.15})_3$	1.2	55	−1000	Negative	25 °C, 20% RH	—	60

the charge transport at the grain boundaries.[194–197] Secondly, considering the significantly lower J_{SC} in their experiment, an excess of positive Na^+ can be easily accumulated within or at the interface of the ETL, impeding its correct operation in the solar cell by generating recombination centers.

Carolus *et al.*[38] concluded that PID significantly dominated any potential benefits of Na^+ diffusion in perovskite solar modules, such as enlargement of the perovskite grain size, passivation of the grain boundaries, and improving the charge transport, as described by Bi *et al.*[197] and discussed earlier in Section 5.3. However, in this specific situation, the opposite impact was also observed, which is not surprising when considering the characteristics of ionic conduction. Evidently, the PSCs used in their system exhibited a reversible form of PID (Fig. 4(c)). After 72 h of being subjected to the same environmental circumstances, switching the polarity of the high-voltage source resulted in a P_{max} recovery of 80%. A recovery of 86% in J_{SC} was the major source of the improvement in P_{max}, which also originated from the increase of 4% in FF, while the V_{OC} remained almost unchanged (1% decrease). Overall, a non-recovered degradation of 15% was found in P_{max} during the PID stress and recovery investigations. The FF (dropped by 10%) and J_{SC} (dropped by 8%) were considered to be responsible for the remaining losses, while the V_{OC} showed a slight increase of 3%. The degradation of the reference sample[192] showed that the thermal stress caused morphological deformation of the spiro-OMeTAD HTL; however, this was considerably less evident in the PID sample. Conclusively, these investigations revealed that PSCs are susceptible to PID, and PID may be reversible by tuning the device stack and the reversed polarity indicates a new regenerative feature unrelated to PID. This study lays the groundwork for future research on PID in PSCs, which can lead to their eventual commercialization. However, although they observed that PSCs are vulnerable to PID and provided no further explanation of this phenomenon or its mechanism, they relied on speculation rather than experimental evidence.

Solution-processed and thermally evaporated perovskites differ in terms of film composition due to the possibility of utilizing additives in the former. Thus far, salts, organic molecules, polymers, inorganic nanoparticles, and metal ions have been studied as additives. Additives passivate defects, eliminate hysteresis, enhance the layered microstructure, and stabilize the photovoltaically active perovskite crystal phase, improving the performance more than devices without additives. However, this approach is incompatible with thermally evaporated perovskite layers. Furthermore, the microstructure of polycrystalline perovskites, which determines the device efficiency and stability, is the fundamental difference between the two technologies for depositing perovskite thin films. In PSCs, the grain boundaries are critical for the migration of ions. Larger, uniform, and compact grains are thought to improve the photovoltaic performance, although this is under debate. Vaynzof *et al.*[198] comprehensively discussed both technologies and summarised the microstructure differences in polycrystalline perovskites with different compositions. These findings

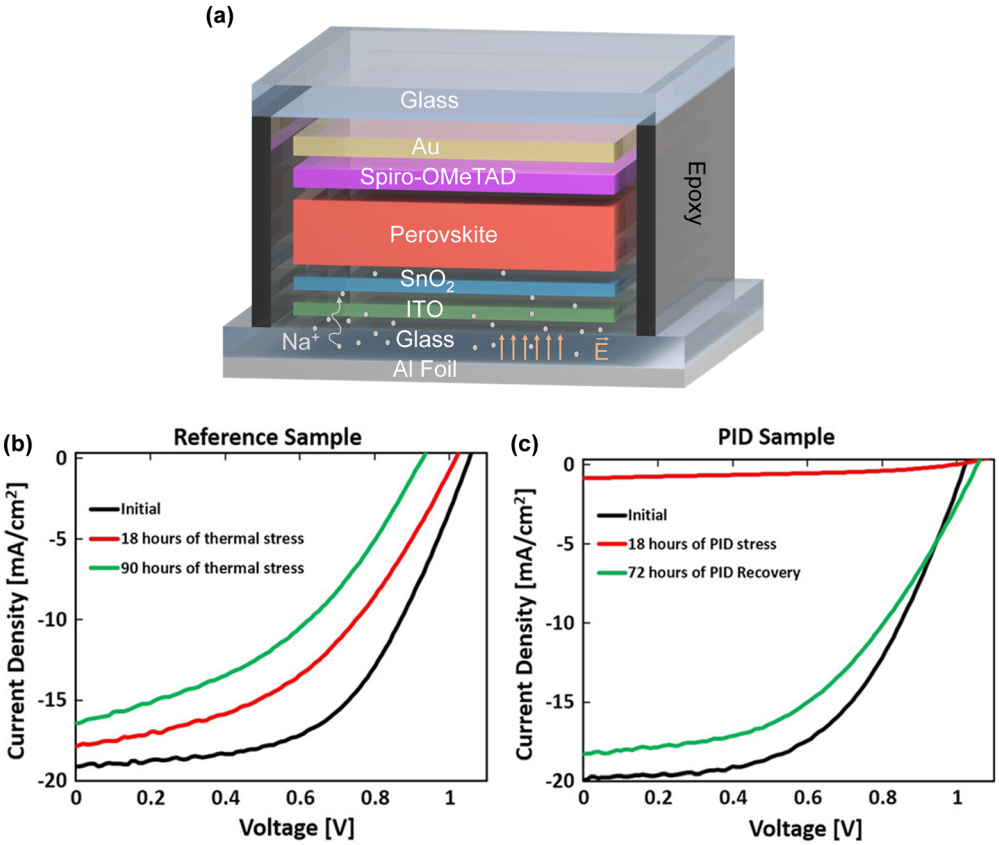

Fig. 4 (a) Representation of an encapsulated n–i–p PSC, where a short-circuit and a high voltage are applied between it and the Al foil on the SLG substrate. (b) *J*–*V* curves of the reference under thermal stress, where no voltage was applied across the reference sample, and the observed degradation was only due to thermal stress. (c) *J*–*V* curves of the PID sample before and after the test. Reproduced with permission.[38] Copyright 2019, Wiley-VCH.

suggest that the grain boundaries can serve as pathways for ion migration during PID.

8.2. PID in PSCs with different architectures

Generally, n-type crystalline silicon solar cells are more sensitive to a positive bias[40,139] than p-type solar cells, which are more sensitive to a high negative voltage bias during PID testing. The PID in negatively biased p-type solar cells primarily comes from the Na^+ ion shunting from the glass cover sheet.[68,70] PSCs have a p–i–n or n–i–p architecture, with perovskite as the absorber layer, ETL (n-type material), HTL (p-type material), bottom contact (metal electrode), and top contact (transparent conducting layer). The light-absorbing perovskite material is sandwiched between the ETL and the HTL. PSCs are particularly susceptible to PID because of the sensitivity of their perovskite absorber to light, temperature, electrical field, oxygen, and humidity, in addition to unwanted ion migration. Carolus *et al.*[38] utilized n–i–p-structure solar cells in their work on PID in PSCs. Following an 18 h PID test conducted at a temperature of 60 °C and RH below 60%, the significant degradation of 95% in P_{max} was detected, which was mostly attributed to the substantial decline of 94% in J_{SC}. It was noted that the degradation was mainly caused by the penetration of Na^+ ions from the SLG. This led to a build-up of ions at the interface with the ETL, which hinders the function of the cell by forming recombination centres. The drop in J_{SC} supports this. The second explanation is the morphological deformation of the spiro-OMeTAD HTL caused by elevated temperature, resulting in deformation under the Au electrode. The 80% recovery observed after reversing the voltage comes mainly from the 80% improvement in J_{SC}. After reversing the voltage, the overall performance recovered by 80%, with the majority of the increase coming from the 80% improvement in J_{SC}. Brecl *et al.*[57] and Nakka *et al.*[59] employed the p–i–n structure to study the PID in PSCs and observed less degradation rates compared to the previously reported PID of n–i–p-based PSCs. These results showed that n–i–p PSCs are more susceptible to PID. In PID testing of PSCs, both terminals of the cell were short-circuited, thus there was no possibility of an electric field between the ETL and HTL. A high electric field only existed between the Al foil on the glass pane and the cell, which forced Na^+ toward the cell from the SLG. The findings by Carolus *et al.*[38] and Brecl *et al.*[57] demonstrated that it is likely that the p–i–n and n–i–p structures are both susceptible to PID, regardless of the composition of the cell.

In early 2021, a detailed study was conducted by Purohit *et al.*[56] on different architecture-based PSCs to investigate their PID mechanism. The different architecture-based solar cells

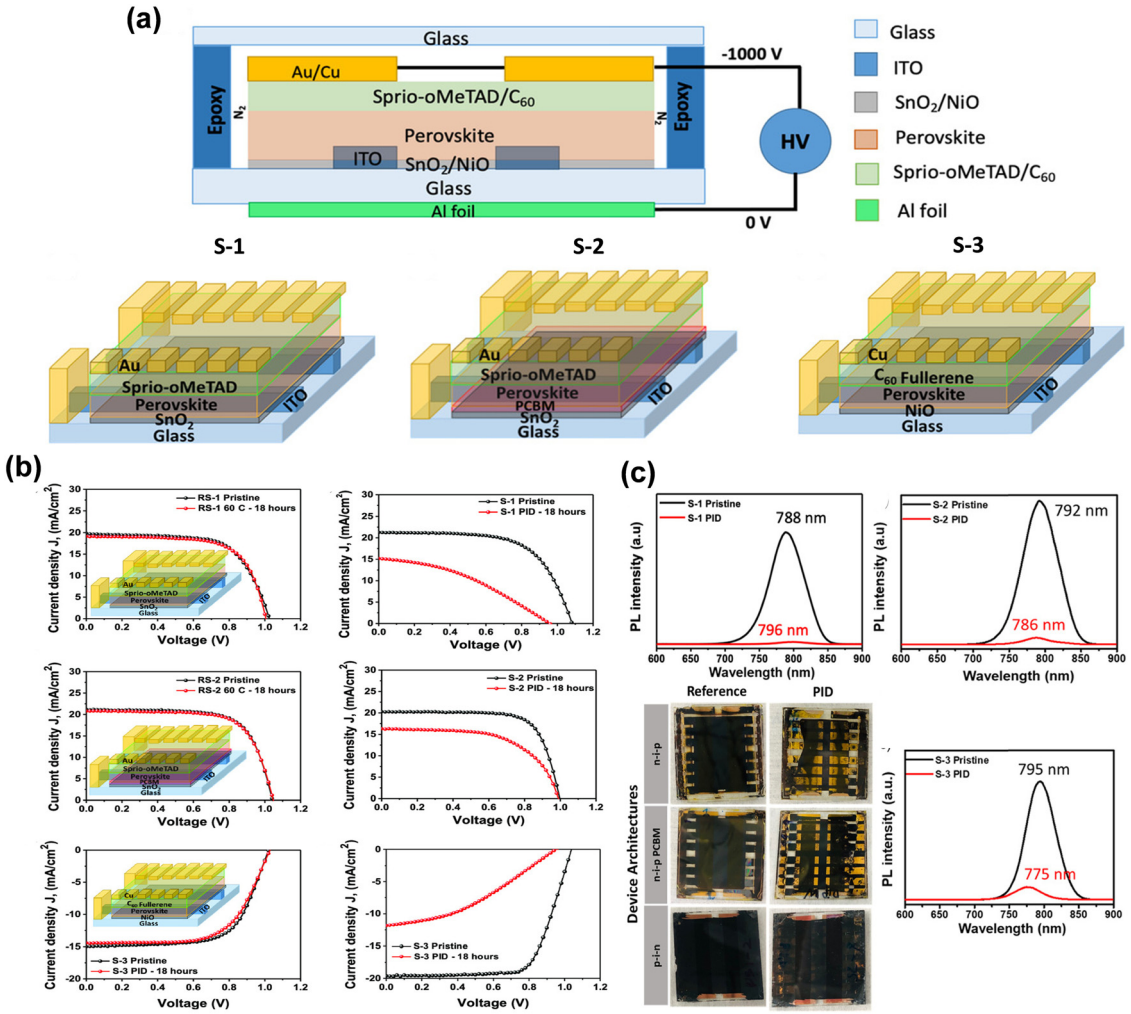

Fig. 5 (a) Schematic interpretation of PID configuration for the three encapsulated PSCs: S-1, S-2, and S-3. (b) *J–V* characteristics of PSCs with different architectures before and after PID and under thermal stress. (c) Optical images of PSCs before and after PID stress with pre- and post-PID photoluminescence (PL) spectra of PSCs of different architectures. Reproduced with permission.[56] Copyright 2021, Wiley-VCH.

used in the study were n–i–p, n–i–p with [6,6]-phenyl-C61-butyric acid methyl ester (PCBM), and stacked p–i–n to investigate the impact of PID on these three different types of PSCs using the foil method. The authors denoted the n–i–p-based PSCs as "S-1" with the configuration of SLG/ITO/SnO_2/$Cs_{0.10}FA_{0.90}PbI_{2.865}Br_{0.135}$/spiro-OMeTAD/Au, n–i–p PSCs with PCBM as "S-2" with the configuration of SLG/ITO/SnO_2/PCBM/$Cs_{0.1}FA_{0.9}PbI_{2.865}Br_{0.135}$/spiro-OMeTAD/Au, and p–i–n-based PSCs as "S-3" with the configuration of SLG/NiO_x/$Cs_{0.18}FA_{0.82}PbI_{2.82}Br_{0.18}$/fullerene ($C_{60}$)/Cu (Fig. 5(a)). The PSCs were encapsulated in a nitrogen glovebox by attaching an SLG to the backside of the cells with epoxy resin. Neither the solar cell nor the resin came into direct contact with the glass at any point throughout the process. To assess the effect of thermal stress at 60 °C, they simultaneously employed three encapsulated solar cells with the designations of RS-1, RS-2, and RS-3 as a reference. For 18 h measurement, a negative potential was applied from the solar cell to the Al foil, which was attached to the front glass (*i.e.*, the SLG substrate).

To further understand PID and thermal stress, they used 30 different sets of PSCs in their experiment. The *J–V* curves of RS-1 are shown in Fig. 5(b) at room temperature and after 60 °C of thermal stress. They found that the PCE dropped from 13.2% to 13% after 18 h of thermal stress, with the losses coming from the 3% relative change in FF, 3% relative change in J_{SC}, and 1.9% relative change in V_{OC}. Alternatively, S-1, which featured an n–i–p stack, exhibited a significantly faster degradation rate due to PID compared to RS-1. Under PID stress for only 18 h, the PCE dropped from 15.7% to 5.4%, with the main contributions coming from a relative change in J_{SC} of 28% and relative change in FF of 45%. The *J–V* curves of RS-2 exhibited a minor change from 15.3% to 15.2% after thermal stress, which was almost stable for 18 h. Fig. 5(b) shows that after 18 h of 1000 V PID stress, the PCE of S-2 degraded from 14.64% to 10%. The p–i–n architecture device of RS-3, as shown in Fig. 5(b), exhibited a steady performance for 18 h under thermal stress, with the PCE dropping from 10% to 9% primarily due to the major relative change of 5% in FF. Furthermore, after 18 h of PID

stress, S-3 degraded noticeably, with a drop in PCE from 14.34% to 4%. All the PSCs showed a massive decline in J_{SC} compared to V_{OC} and other performance indicators when operating under PID. Because of the intrinsic instability that develops under PID, the decreased J_{SC} explains the elevated rate of recombination of the produced excitons in the active perovskite layer.

All the PSCs treated with PID showed decomposition and phase segregation of the perovskite absorber layers after 18 h treatment, which described the inherent instability of the bulk perovskite material (Fig. 5(c)). Mixed halide perovskites based on Cs-FA are reported to be a suitable solution to overcome Br–I photoinduced phase segregation for regular device operation.[199] All the PID-treated PSC samples (shown in Fig. 5(c)) exhibited stable photoluminescence (PL) spectra, indicating a substantial intensity difference compared to the untreated samples. There was a noticeable shift in the peak wavelength from 788 to 796 nm for S-1, and then from 792 to 786 nm and 795 to 775 nm for S-2 and S-3, respectively. The changes in the optical energy bandgap (E_g) reflected significant alterations in the chemical structure and stoichiometry of the perovskite absorber layer resulting from PID. The blue shift reflected a change in the Br/I composition, which is abundant in Br for S-2 and S-3. The majority phase lost Br for S-1, which was reflected by the increased quantum yield, as seen in the redshift in its spectrum (Fig. 5(c)).[200] The intrinsic instability of ionic bonds under PID is related to the observed properties of weak ionic bonds of ionic conductors, soft lattice structure, and van der Waals interactions and the bond energy of Pb–I is around 142 kJ mol^{-1}. Alternatively, the bond energy of silicon is substantial with a value of 222 kJ mol^{-1}, indicating that its covalent bonds are particularly robust. However, due to the low activation energy of the ionic components in PSCs, their migration under a strong potential is easy, resulting in the undesirable ion redistribution inside the absorber layer, which is the opposite of that in silicon solar cells, where PID causes Na^+ to migrate from the SLG. The significant effects result from ion migration and redistribution, including halide segregation (Hoke effect), cation segregation, and photodecomposition.[201–206]

In addition, it was suggested that ion migration generates intrinsic defects, such as vacancies, interstitials, and anti-site defects, which provide an abundance of trap states in the absorber layer and at the interfaces, boosting the nonradiative recombination, and eventually causing the device to fail under PID. Comparatively, S-2 with the additional PCBM layer degraded less than S-1 and S-3. An important change in electronic characteristics was observed when PCBM was incorporated as one of the layers in the PSCs. It was observed in numerous investigations that the Pb-I anti-site defects, iodide ions, and defects are entrapped by binding the PCBM molecules in the bulk of perovskite.[207–209] Ion movement or vacancy occupation are both impeded by the PCBM layer, which is also seen to serve as a physical barrier. Another possible explanation for the slight suppression of the PID effect in S-2 is that PCBM has a high activation energy, indicating that more energy is required to drive extrinsic or internal ions than in the common perovskite when subjected to an external electrical field.

Given that the role of ion migration in all PSCs is still unclear, Purohit *et al.*[56] proposed that the following reasons may explain the degraded performance of PSCs due to PID. In particular, the weak ionic bonds cause facile ion migration, resulting in the undesirable phase segregation and decomposition. The presence of intrinsic and extrinsic defects under PID increases the nonradiative recombination *via* trap states within the absorber layer and/or at the interfaces. All three stacks were tested and shown to be susceptible to PID, whether they contained n–i–p, n–i–p PCBM, or p–i–n-based PSCs. Nevertheless, compared to solar cells based on PCBM and the other two stacks, that based on n–i–p PCBM showed much less degradation. The comparative study demonstrated that the PID and stability issues of PSCs are the main issues that may arise on large-scale installations in the real field. Considering that understanding the mechanisms of its degradation is crucial to the long-term stability of perovskite PV technology, these findings can help future research in this area.

8.3. PID of PSCs under different voltages

Brecl *et al.*[57] compared two different bias voltages, ±500 V (half of the current system voltage) and ±1000 V, by performing standard *I–V* and EL tests. The devices exhibited a considerable PID resistance at the bias voltage of ±500 V, which was significantly higher than the silicon PV-specific recommendations. Moreover, time-of-flight secondary ion mass spectrometry (ToF-SIMS) measurements of the depth and spatial distribution of elements in solar cells revealed a quick degradation of the bias voltage of −1000 V due to the entry of Na^+ from the glass substrate. The positively biased devices were not significantly affected by prolonged exposure to high voltage. Given that there is no set of standard certification tests for PID of PSCs available to date, they followed the procedures used for crystalline silicon PV modules, which involved wrapping the module in a conductive foil and subjecting it to PID testing for 168 h in a controlled environment. Before and after the test, the external quantum efficiency (EQE) of the tested module was evaluated, and certain samples were analyzed using ToF-SIMS to determine whether the Na^+ penetrated across the device. The tested devices, with an inverted (p–i–n) structure, were fabricated using MeO-2PACz as the HTL (to make the cells more stable) and C_{60}/SnO_2 as the ETL, in addition to an efficient and stable triple cation perovskite absorber layer.[79,210] The cells were sealed with a two-component epoxy edge sealant and a cover glass and the average surface of the device area was about 1 cm^2. They used an in-house built setup to check the PID of PSCs, in which all the cells were soldered on a printed circuit board and covered with a conductive plate, and their top was wrapped with Al foil to facilitate better contact with the glass. Moreover, to improve the contact, the entire stack was compressed according to IEC 62804-1.

A bias voltage was applied to the cell by short-circuiting its positive and negative terminals, and the conduction plates surrounding the cell were grounded, as shown in Fig. 6(a).

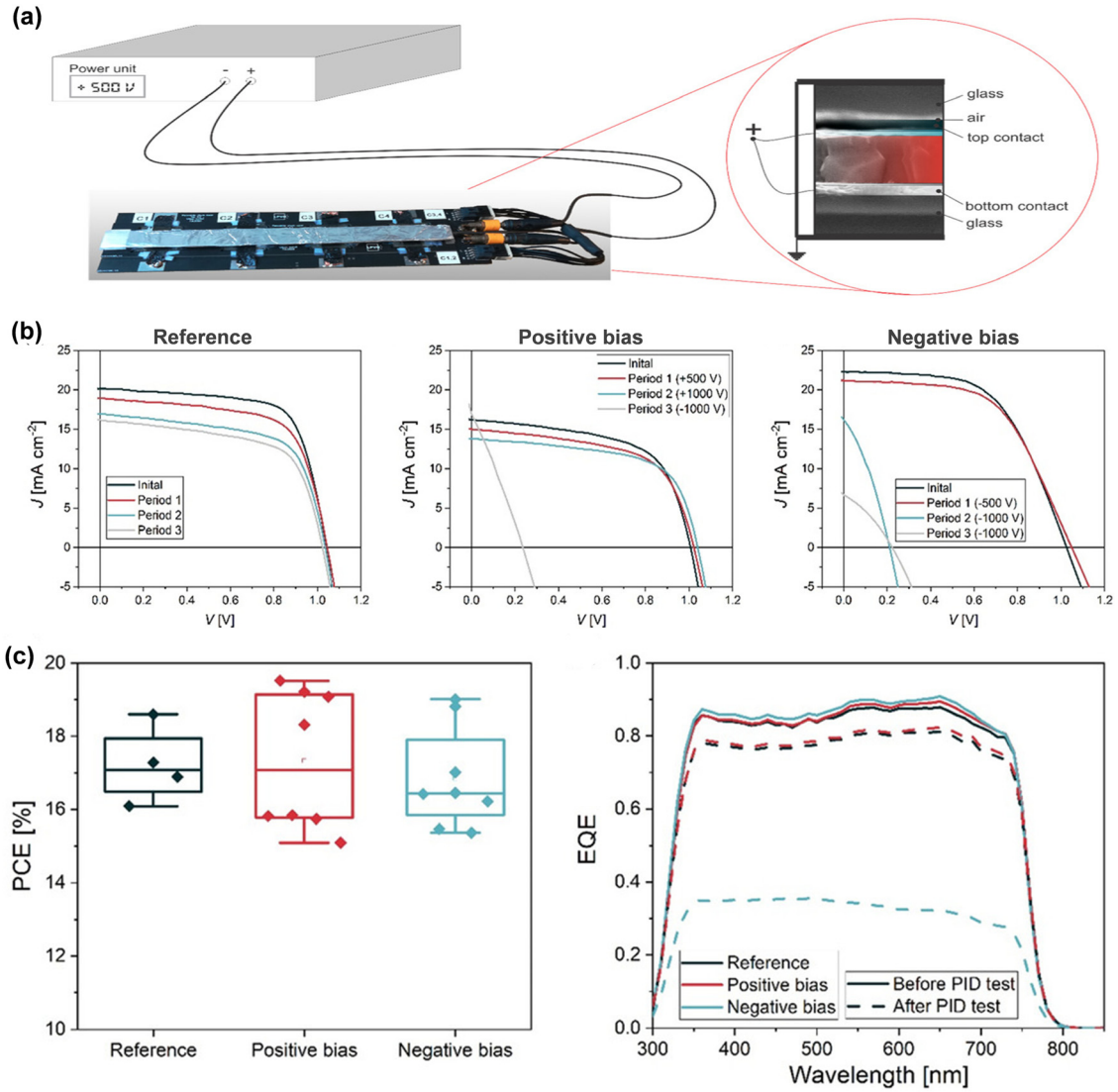

Fig. 6 (a) Prior to PID testing, the PCE of a few selected devices. Comparison of the average EQE of devices in each circumstance before (solid lines) and after (dashed lines) PID test. (b) *J*–*V* curves of the reference cell and PSCs with a positive and negative bias. The initial *J*–*V* curve (black line), the curve at 500 V bias voltage before increasing it to 1000 V (red line: period 1), the curve before changing the voltage from −1000 to 1000 V (cyan line: period 2), and the curve after the test when the devices under test were all at 1000 V (grey line: period 3). (c) PID testing setup. A selected device cross-sectional SEM image at higher magnification is shown in the circle in a. Reproduced with permission.[57] Copyright 2022, Wiley-VCH.

However, when the PV modules in the string were not grounded, they were exposed to a potential range of −500 V to +500 V with respect to the grounded frame; additionally, the solar cells were kept in the dark, and the bias voltage used in the experiment was equivalent to the 1000 V typically used in PV systems. A set of 20 PSCs was used for the investigation, where eight were given a positive bias, eight were given a negative bias, and four were kept unbiased in the dark as the control. The bias voltage was raised to 1000 V after 112 days, and the positively biased solar cells were connected to a negative bias with the same magnitude after 196 days. Overall, the cells were subjected to high potential for about 200 days or 5000 h, which was significantly longer than the minimum test period required for silicon modules (168 h). *I*–*V* and EL measurements, which required disconnection of the devices from the bias during PID testing, have been used frequently to examine the device performance. Initially, a 3-day measuring interval was used to observe any potential rapid degradation, which was further increased to 14 days and maintained throughout the test.

The major impacts of PID were studied with ten sets of *I*–*V* measurements for each device (many measurements were required because the first few readings showed a significant improvement in V_{OC} under light soaking). Additionally, a few of the devices even exhibited a slight drop in J_{SC} together with an increase V_{OC}. The performance of all devices degraded throughout the tests; however, the devices subjected to a negative voltage bias of 1000 V showed the most noticeable loss of performance in V_{OC} (Fig. 6(b)). Before and after the PID test, the EQE measurements corroborated this pattern, revealing a negligible decrease for the reference and positively biased solar

cells (Fig. 6(c)). However, the decline was more pronounced for the negatively biased devices, with the EQE decreasing by more than 50% across the whole wavelength range.

Additionally, EL images offered more evidence and demonstrated that similar to the *I–V* measurements, the most obvious pattern was the failure of EL emission, which is correlated with the significant drop in V_{OC}. Among the eight negatively biased cells, seven failed at 1000 V, and one failed at 500 V, with a total failure rate of 100% for the negatively biased group. The EL of the initially positively biased cells did not degrade under positive bias; however, when they were exposed to a negative bias of 1000 V, six of the eight cells failed, one cell started degrading, and one cell did not degrade at all, resulting in a failure rate of 75%. Among the four reference cells, three did not degrade, while one degraded very slowly after 161 days. The typical EL images were recorded during the experiment, as shown in Fig. 7(b), depicting the device operated at various stages of testing after it was initially linked to the positive bias. The EL signal immediately began to drop when the device was connected to the negative bias (−1000 V). Large inhomogeneities arose, covering 20–80% of the cell surface area, which exhibited a significant decrease in EL emission (Fig. 7(a), all panel figures). However, additional studies are required to validate and determine the causes of the inhomogeneity, while the data suggest approaching cell failure due to the PID. Using the ToF-SIMS technique, they detected the presence of numerous Na-based ions combined with iodide and bromide, such as NaIBr (Fig. 7(c)). However, it was unclear whether these ions were produced by the Na reactivity with halide ions inside the device or by-products. The devices were rapidly degraded after being subjected to a negative bias of 1000 V, as evidenced by both the *I–V* and EL findings. In contrast, neither the +500 V, +1000 V, nor the −500 V biases exhibited any noticeable effect.

8.4. PID of PSCs under different thermal stress

In 2023, Nakka *et al.*[59] conducted a study on glass-encapsulated PSCs under two different thermal stress conditions for 55 h, *i.e.*, room condition (RC) (25 °C with 20% RH) and elevated stress conditions (ESC) (60 °C with 60% RH). They used glass-encapsulated p–i–n structures with the configuration of ITO/self-assembled monolayer (SAM)/triple cation CsFAMA absorber layer/C60/BCP/Ag solar cell. The devices subjected to a negatively biased PID exhibited significant and rapid degradation under ESC, retaining only 10% of their initial PCE. Conversely, the devices under RC demonstrated better tolerance to PID, retaining 41% of their initial efficiency. Partial recovery of degradation was observed in the RC devices through the application of a reverse bias (+1000 V), whereas minimal recovery was observed in the ESC devices. The magnitude of PID was influenced by ESC, and simply reversing the polarity was insufficient for PID recovery. To investigate and comprehend the behaviour and mechanisms responsible for PID in their solar cells, various analyses such as light and dark *I–V*, EQE, PL, photoluminescence quantum yield (PLQY), and XRD were performed.

The initial average absolute PCE of the glass-encapsulated devices was 19.6%, increasing to 20.1% after 55 h of storage in an N_2 environment. Under biased conditions at −1000 V for 55 h, the efficiencies reduced were by 59% compared to the controlled devices. The decrease in PCE primarily resulted from the reduction in J_{SC} by 27% and FF by 36% (Fig. 8(a)). In the case of the negatively biased PID devices, the steeper slopes in the dark *I–V* characteristics indicated a lower shunt resistance and higher leakage current. These devices exhibited a 40% reduction in EQE compared to the controlled devices (Fig. 8(c)). The recovery experiments with a reverse bias of +1000 V for 90 h showed an improved device performance from 37% to 58% for the PCE of the control device, with J_{SC} and FF improving to 83% and 77% of the reference values, respectively, indicating partial recovery (Fig. 8(a)). Alternatively, they also conducted an experiment using the same procedures under ESC to investigate whether the behavior of PID in PSCs depends on the operating conditions. The initial average absolute PCE of the glass-encapsulated solar cells subjected to ESC for 55 h without any voltage stress was 18.5%. A loss of 7% in normalized PCE due to ESC alone was observed without applying any voltage stress. However, when subjected to a high negative bias under ESC, more than 90% PCE was lost compared to the controlled devices in 55 h. This loss was significantly higher than that (59%) observed under the reverse bias conditions (Fig. 8(b)). The dark *I–V* curves of the ESC devices showed a high leakage current, reaching 58.0 mA cm^{-2}. Additionally, the devices with negatively biased PID under ESC exhibited a 60% reduction in EQE compared to the control devices (Fig. 8(d)). The recovery experiments by applying a reverse bias of +1000 V for 90 h resulted in only a 10% recovery in PSC for the ESC devices (Fig. 8(b)). The results highlighted the stronger PID effects in the devices stressed under ESC compared to that stressed under reverse bias. These results demonstrate that negative biasing or negative PID is more decisive for devices than positive PID, which is consistent with prior studies on the PID of PSCs. Furthermore, the elevated thermal environment speeds up the degradation process. Also, the device performance recovery under different environmental circumstances also revealed that degradation under negative biasing is less recoverable because the ion migration cannot be reversed completely.

To investigate the underlying mechanism for PID in their devices, they performed PLQY spectroscopy. The PL peak intensity of the majority of the solar cells occurred at around 736.7 ± 0.2 nm, except for the negatively biased PID solar cells (Fig. 8(c)). Under RC, the solar cells with negatively biased PID showed a PL peak with a redshift of approximately 8 nm and significant quenching of more than 50% in PL intensity. This indicated the formation of iodine-rich regions and nonradiative recombination. Under ESC, the solar cells without high voltage stress showed a minimal redshift of 1 nm, whereas the devices with negatively biased PID exhibited a redshift of 22 nm and 62.5% quenching in PL intensity. The PL results were consistent with the analysis of the *I–V* characteristics. The recovery under reverse bias showed partial recovery, as indicated by the blue shift in the PL peak position and partial enhancement in

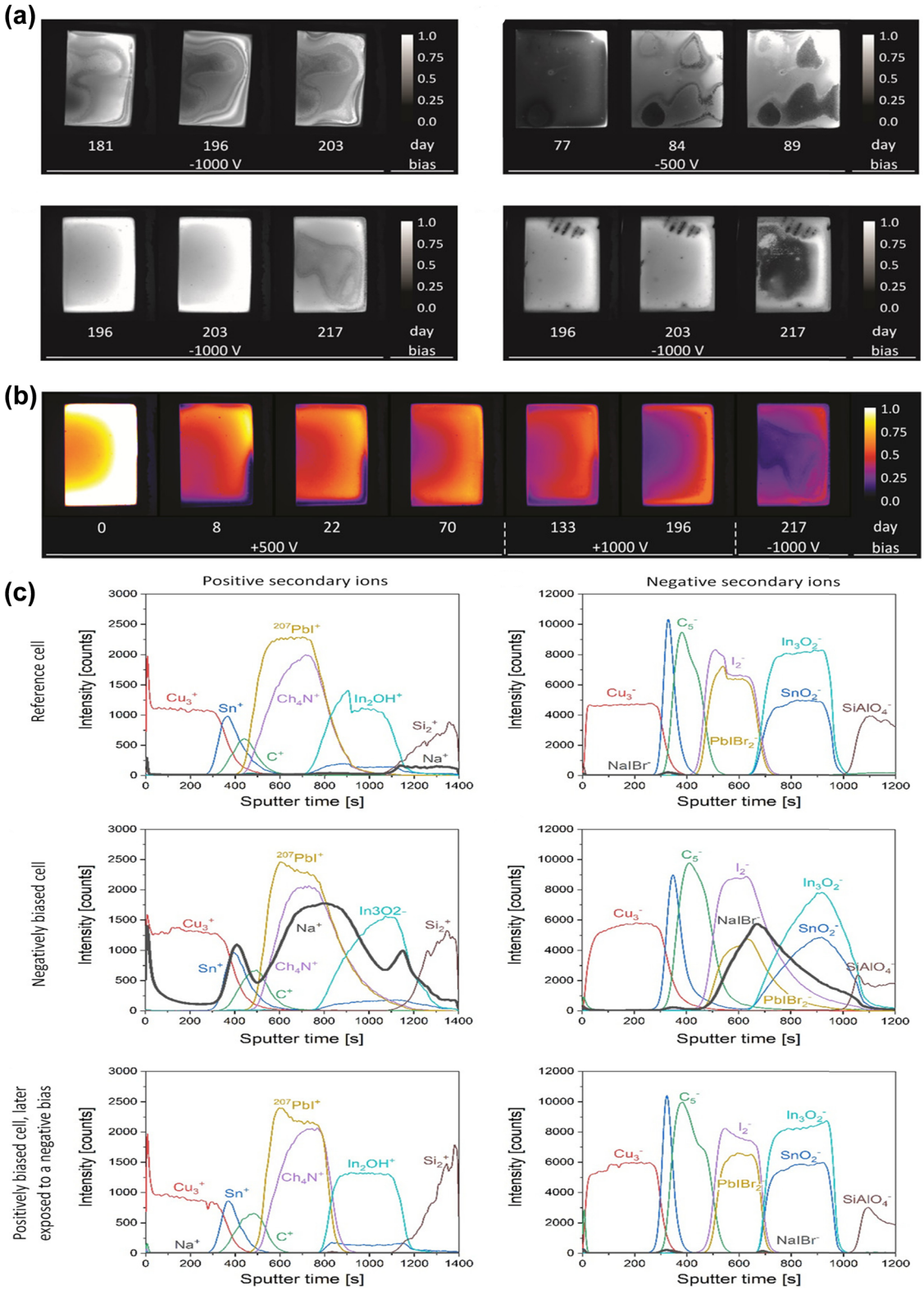

Fig. 7 (a) Individual normalized EL images with a particular form of inhomogeneity that established itself just before failure owing to the cells subjected to a negative bias, cells subjected to a positive bias, and cells subjected to both biases. (b) EL images of a chosen cell stabilized at a rated J_{SC} on days 0, 8, 22, and 70 at +500 V bias; days 133 and 196 at +1000 V bias; and day 217 at −1000 V bias. (c) ToF-SIMS depth profiles of secondary ions (positive on the left and negative on the right) for a reference cell, negatively biased cell, and negatively biased cell subjected to a positive bias. Reproduced with permission.[57] Copyright 2022, Wiley-VCH.

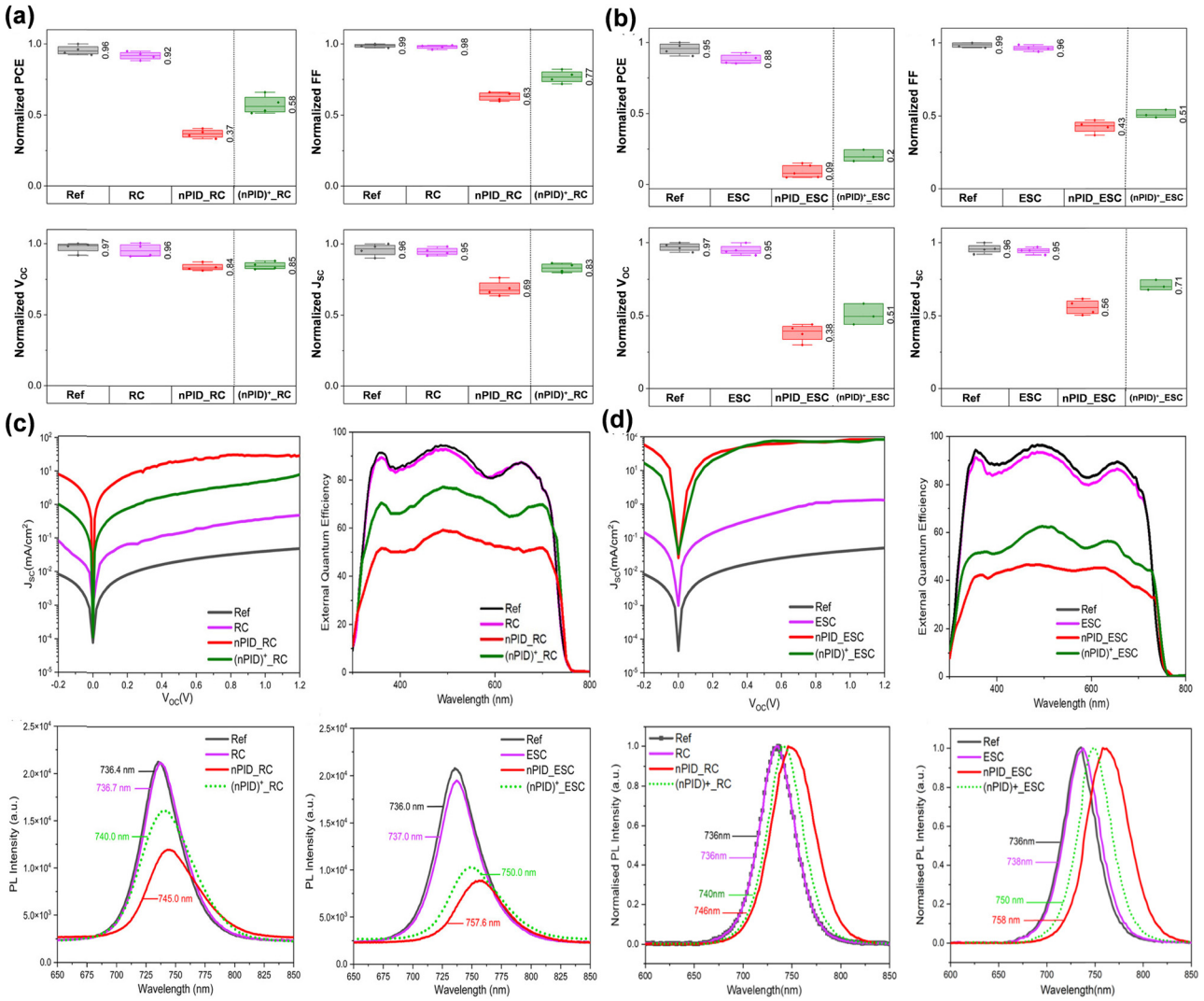

Fig. 8 (a) *J*–*V* parameters under RC. (b) *J*–*V* parameters under ESC. (c) Dark *I*–*V* curves and EQE under RC. (d) Dark *I*–*V* curves and EQE under ESC. Reproduced with permission.[59] Copyright 2023, Wiley-VCH.

PL intensity. However, under ESC, the PL peak position remained different from the controlled devices, and the recovery of the PL intensity was much weaker, indicating poor recovery. These findings suggest that negative high voltage stress led to more iodine-rich regions and increased the nonradiative recombination, which were further exacerbated under ESC.

Also, XRD characterization was performed to study the degradation of PSCs under PID stress (Fig. 9(a) and (b)). Under RC, the solar cells with negatively biased PID showed a weakened intensity of the perovskite peak (14.2°), indicating their degradation. Additionally, the peaks corresponding to halide segregation (PbI_2 peak at 12.54°) and ion migration (AgI peak at 38.2°) in the absorber layer were observed in these devices. Similar results were observed under ESC, with an increase in the intensity of the PbI_2 and AgI peaks. The application of a reverse bias partially recovered the perovskite peak intensity but did not eliminate the undesirable PbI_2 and AgI peaks. The recovery was more limited for ESC due to the stronger decomposition of the perovskite. Negative high-voltage bias had a detrimental effect on the PSCs, resulting in catastrophic failure, particularly under ESC.

The SEM images of the PSC stack showed that the control devices did not exhibit Na^+, even in the ITO layer (Fig. 9(c)). However, the devices subjected to a high negative voltage bias displayed a high concentration of Na^+ in the perovskite layer, indicating the migration of Na^+ from the SLG. EDX characterization confirmed the movement of Na^+ towards the perovskite layer during negatively biased PID, resulting in the formation of weak Na^+I^- bonds (Fig. 9(c)). At the rear surface of the solar cell, the presence of Ag^+ ions from the rear contact and the formation of a strong AgI bond were observed under both RC and ESC. Recovery through reverse bias in RC led to a reduction in Na^+ concentration, while the AgI peak remained unchanged, suggesting partial recovery. ESC exacerbated the PID, resulting in an intensified PbI_2 peak and a redshift in the PL peak. The

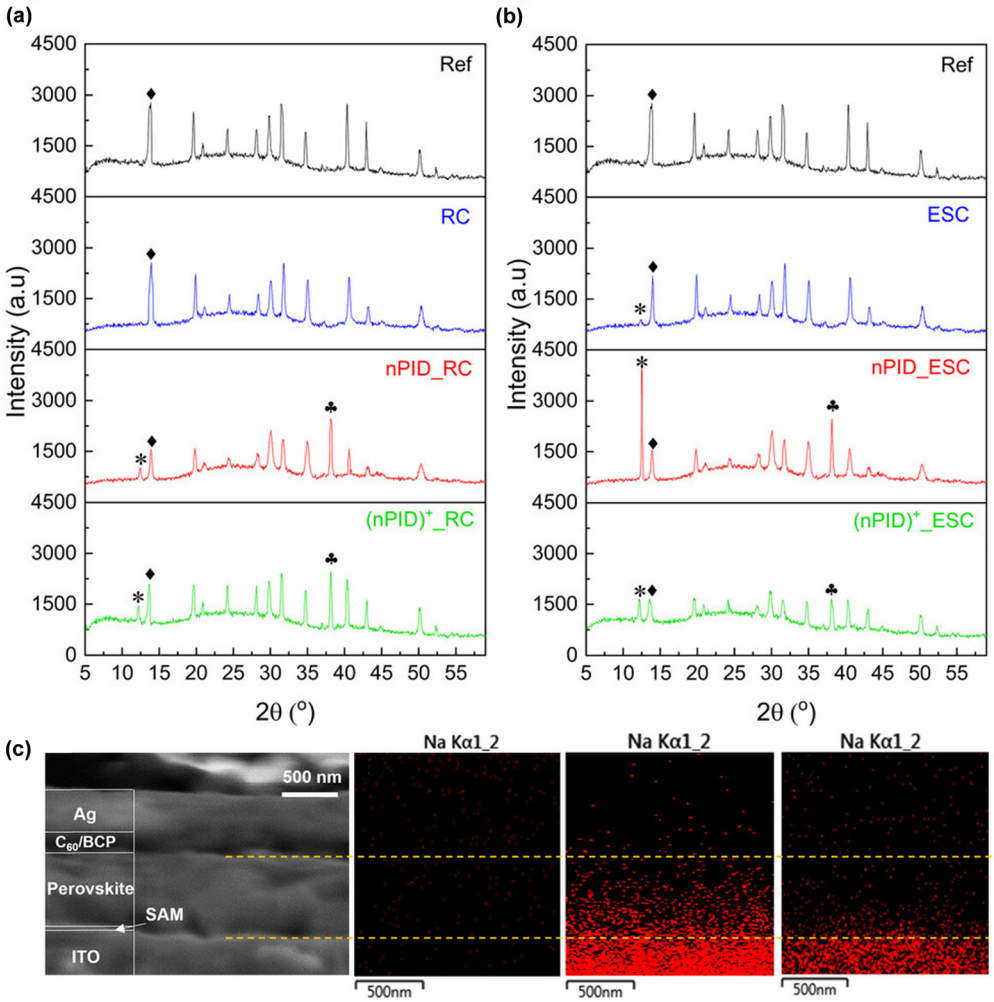

Fig. 9 (a) XRD under RC. (b) XRD under ESC. (c) SEM image of PSC and EDX images of Na^+ mapping of reference under RC, under PID with negative biasing, and recovered devices. Reproduced with permission.[59] Copyright 2023, Wiley-VCH.

application of reverse bias did not fully restore the devices, and the AgI and PbI_2 peaks persisted.

This work provided a more detailed study of the PID in PSCs compared to the existing literature. Different characterization techniques were used to investigate the PID phenomena thoroughly, and the arguments were supported with experimental evidence. A series of experiments demonstrated that the working environment influences the PID in PSCs. Elevated temperature and humidity conditions were more damaging for the PSCs under high voltage. They confirmed the significant role of Na^+ ions in decreasing the device performance under PID stress, as observed in other PV technologies. However, additional non-recoverable stability-related concerns with PSCs impacted their performance under the PID test even more, and the application of reversed biasing was not sufficient to completely recover the degraded devices.

8.5. Role of barrier layer and mitigation of PID in PSCs

Integrating effective barriers in PSCs is equally important as enhancing the perovskite layer and establishing robust external device encapsulation/packaging technologies for long-term device stability. These barriers protect the critical perovskite layer and other functional layers from heat, light, and H_2O/O_2, as well as ion/molecular and diffusion/volatilization. PSCs are unstable owing to the degradation of the perovskite and functional layers due to external stressors such as oxygen, moisture, heat, light, and electric bias.[211] Degradation processes in PSCs may be complex due to the distinct effects of numerous stressing elements on each functional layer. Introducing barrier layers is a technique employed to enhance the long-term stability of PSCs. These barriers can be integrated at all the interfaces of PSCs, including organic or inorganic barriers with a dense structure and strong shielding properties at the charge transport layer/perovskite or charge transport layer/electrode interfaces, as well as UV filtering barriers at the TCO side. A comprehensive overview concerning the employment of barriers was presented in our previous work.[212]

In recent studies about PID in PSCs, Purohit *et al.*[56] and Nakka *et al.*[59] employed PCBM and NiO_x barrier layers to mitigate PID. Purohit *et al.* observed that the PCBM layer serves

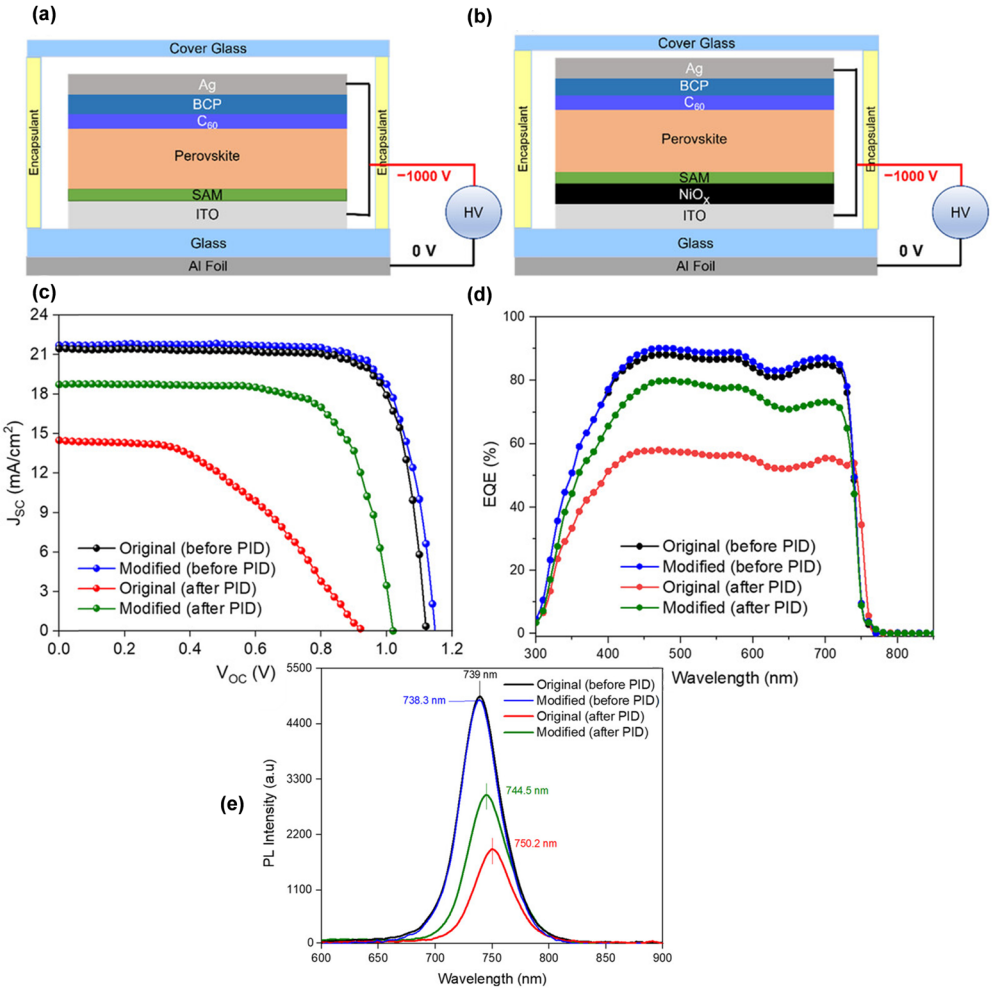

Fig. 10 (a) and (b) Schematic representation of the cross-sectional PSCs and PID setup. (c) *J–V* curves for reference and target PSCs before and after PID test. (d) EQE results of reference and target devices. (e) PLQY results of reference and target devices. Reproduced with permission.[60] Copyright 2023, Wiley-VCH.

as a physical barrier, preventing ion migration or occupying vacancies. Furthermore, PCBM has a high activation energy, suggesting that it requires more energy to move extrinsic or internal ions compared with standard perovskite when subjected to an external electrical field. This can be one of the factors contributing to the partial suppression of the PID effect. Nakka *et al.*[60] conducted a detailed study to mitigate the effects of PID using NiO_x between the SAM and perovskite layer to block the diffusion of Na^+ ions. They used a similar setup as discussed in the previous section in detail. The schematic diagrams of the devices are shown in Fig. 10(a) and (b). Here, the stress duration of the high voltage disparity extended to 96 h according to the test standards used for commercially available PV technologies but under room conditions. A 27% retention in initial PCE was observed in the devices without NiO_x after PID stress. However, an increased retention (65% of initial PCE) was observed after using an NiO_x layer to block the diffusion of Na^+ ions, which is considered the significant cause of PID. The *J–V* curves of their reference and target devices before and after PID stress are shown in Fig. 10(c). A significant reduction in the performance of the reference devices was observed due to the reduced J_{SC} and FF. However, the target devices showed a better performance due to a lower reduction in J_{SC} and FF after PID stress. The *J–V* results were supported by the EQE results, where the reference devices showed a reduction of 35% and less than 20% in the target devices, as shown in Fig. 10(d). In the PLQY measurements, the PL intensities of the reference and target devices were around the wavelengths of 739 and 738.3 nm, respectively, without applying high voltage, as listed in Fig. 10(e). After undergoing the PID test, reference device showed a quenched PL peak at around 750.2 and target device at around 744.5 nm, respectively, which indicated the reduction in non-radiative recombination. The overall performance of the target devices was much better than the reference devices in the PID test.

Mitigation of PID was done by controlling the diffusion of Na^+ ions through the introduction of an NiO_x layer. It was clearly evidenced from the EDX and XRD analysis (Fig. 11(a) and (b), respectively) that the introduction of an NiO_x layer between the ITO and SAM reduced the diffusion of Na^+ ions

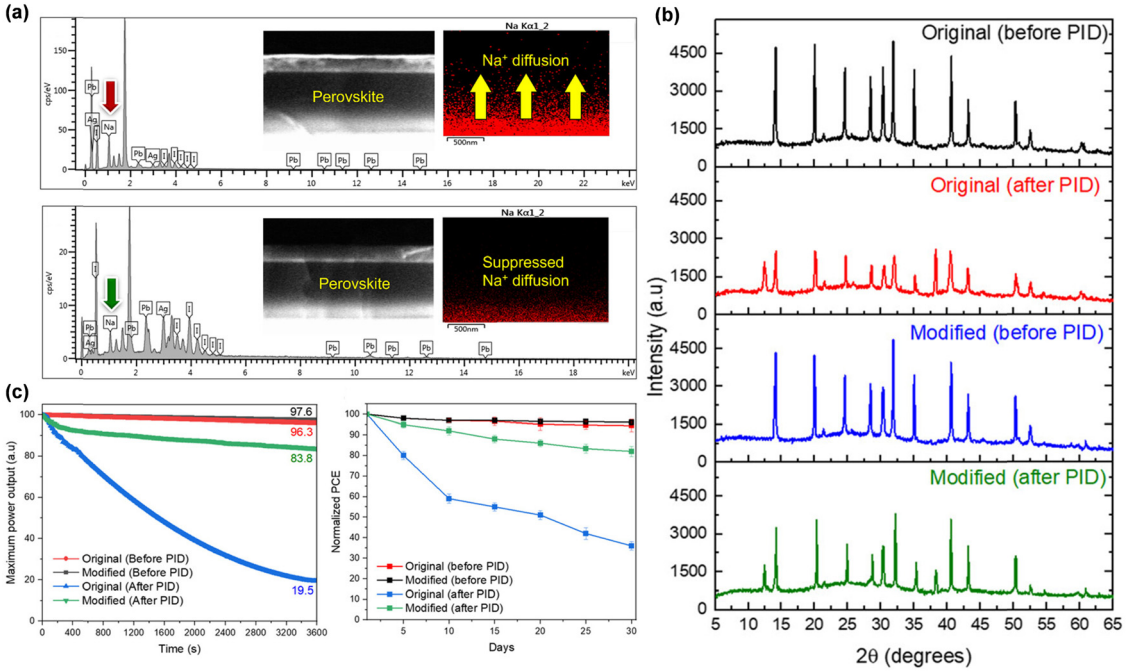

Fig. 11 (a) EDX analysis before and after PID test for the reference and target devices. (b) XRD comparison of reference and target devices before and after PID test. (c) Stability-related data for the reference and target devices. Reproduced with permission.[60] Copyright 2023, Wiley-VCH.

through the SLG into the perovskite layer after performing the PID test. Furthermore, they optimised the thickness of the NiO_x layer to achieve a better performance and PID resistance, which was 50 nm. Moreover, the stability studies after PID test were also conducted in a nitrogen glove box in the dark for the reference and target devices (Fig. 11(c)). The target devices showed more stable behaviour after the PID test. Here, in this study, the PID was not fully mitigated but it paved a way toward the mitigation of PID, which will finally participate in the commercialization of PSCs. Regarding a perfect barrier design and fabrication to overcome PID in PSCs, it was suggested that a perfect barrier film should have the following properties: (i) be intrinsically stable under light, thermal, humidity/oxygen, and electric bias, (ii) low reactive with adjacent functional layers, (iii) highly crystalized, defect-less, and morphologically compact and (iv) have excellent self-resistance to PID, especially for ion migration under PID.

8.6. PID in perovskite-based tandem solar cells

The theoretical radiative efficiency limit for a single-junction PSC with a bandgap in the range of 1 to 1.5 eV is 31%, according to the Shockley–Queisser model, which can be surpassed using multi-junction cells. With their tuneable bandgaps and outstanding optoelectronic capabilities, perovskite materials can be used in TSCs in combination with organic solar cells, CIGS, silicon, and others. However, the performance and prospects of these materials are still hampered by various degradation mechanisms, some of which are primarily intrinsic. For instance, the ionic properties of perovskite materials promote ion migration and redistribution. This process results in the generation of intrinsic defects and various effects such as halide segregation, cation segregation, and photodecomposition. Consequently, the long-term stability of the perovskite material is diminished. The stability problems of perovskite-based tandem devices primarily arise from the degradation of the perovskite films when exposed to water, oxygen, heat, and light. Thus, to enhance the device stability, it is crucial to produce high-quality perovskite films, based on minimal grain boundaries and defects. This approach can effectively mitigate the detrimental effects of water and oxygen erosion.

In the case of perovskite–perovskite TSCs, typically, a high Br ratio (>40%) is needed to achieve a wide-bandgap (1.8 eV) top cell, resulting in increased trap density and severe phase segregation.[213,214] Incorporating Sn^{2+} in the bottom cell composition provides a stability concern due to its susceptibility to oxidation, resulting in the formation of Sn^{4+}.[215] Currently, realizing stability in perovskite-perovskite TSCs is challenging and in its early stages of optimization.[216] Alternatively, CIGS, popular thin-film solar cell technology, combines well with perovskite due to its narrow and tunable bandgap.[152] In this case, the roughness of the interconnecting layers is crucial to the performance of perovskite/CIGS tandems, which offer benefits in terms of compatibility with solution processing and low-cost manufacturing. However, an obstacle for monolithic tandem integration in CIGS is that the maximum vertical distance of the top surface of the subcell is comparable to the thickness of the perovskite layer.[217] Perovskite–OPV tandems have gained attention due to enhanced stability and efficiency, notably with the development of non-fullerene acceptors for OPV.[218,219] OPV is a solution-processable method that minimizes damage to the superstrate-formed perovskite cell when manufactured in a nonpolar solvent. The perovskite–OPV

tandem can be manufactured by the roll-to-roll technique for flexible applications.[220] Perovskite/Si tandems exhibit a higher performance level than other materials for Si-based tandem applications. They have a tunable optical bandgap ranging from 1.5 to 1.75 eV, which is suitable for both two-terminal and four-terminal Si tandem configurations.[221,222] Furthermore, the perovskite absorber and its charge transport layers can be applied utilizing uncomplicated, inexpensive manufacturing techniques that can adapt to textured surfaces.[223,224]

However, the main difficulty encountered by perovskite-based tandems is that these devices not only face the inherent stability issues of PSCs but also have additional obstacles specific to the tandem arrangement, such as charge transport layers, encapsulation methods, and operation circumstances.[225–228] The absence of a standardized stability test technique for tandem devices further complicates the direct comparison of the stability results, impeding the understanding of fundamental degradation mechanisms.[229] Recently, several routes on three levels have been released to improve the stability, as follows: (a) perovskite materials degrade easily when exposed to oxygen, moisture, and heat, and hence, TSCs need an appropriate device stack and encapsulation to prevent degradation. The intrinsic stability of pristine absorber materials can be improved by eliminating bulk ionic defects, passivating the grain boundaries and surfaces, and providing hydrophobic perovskite surface treatments. Additives enable bulk defect reduction.[230,231] (b) Charge extraction and degradation-resistant contact layers increase the device stability. Here, metal oxides from atomic layer deposition (ALD) and sputtered layers[232,233] are better than metals that diffuse or react with the absorber.[234] Thick metal oxide layers avoid moisture and breakdown product effusion.[232] (c) The glass/glass sheets and UV-curable adhesive adequately encapsulate single and TSCs.[235,236] However, ethylene-vinyl acetate may not work given that acetic acid damages perovskite, and thus appropriate encapsulation with encapsulants is needed.[235,237] In this case, to realize the commercialization of perovskite-based TSCs, it is necessary to satisfy the requirements of the PID test. The stability of the majority of perovskite-based TSCs is now undergoing a challenging phase. Currently, there is no accessible literature regarding the PID in perovskite-based TSCs, with the exception of perovskite/Si TSCs.

Xu *et al.*[58] fabricated a module that closely resembled a commercially available module and conducted a study to examine the effects of high voltage on the perovskite/silicon TSC (PVSK/Si TSC).[238] Thermoplastic polyurethane (TPU), a popular insulating material, was employed as an encapsulant between the glass layers that held the PVSK/Si TSC (Fig. 12(a)). Subsequently, the PID was investigated by wrapping the module in Al foil and subjecting it to a $\pm$1000 V bias at 60 °C, which simulated the actual working circumstances. Multiple samples were employed in the experiment, each of which was subjected to a unique series of stresses (including negative and positive potential and thermal operation, which are performed in an N_2 atmosphere with or without light biasing). Then, the PV parameters such as FF and PCE were evaluated, and PID was found to be present in the PVSK/Si TSC.

The study revealed that under the operating conditions, a positive potential has no significant detrimental effect on cells compared to thermal stress. However, a negative potential can lead to the rapid degradation of cells within a few hours. After exposure to 1000 V for 24 h, the power conversion efficiency (PCE) of the module decreased to 50% of its initial value. The EL images and PL spectra of the negative-PID (n-PID) were further studied to differentiate the responses of the subcells (Fig. 12(b)). Most of the PVSK/Si TSC failure occurred in the perovskite subcell. Although the Si subcell experienced slight damage, it was largely recoverable through the application of a positive bias. Through elemental analysis conducted using secondary-ion mass spectrometry (SIMS) and transmission electron microscopy (TEM), it was observed that unlike the single-junction cases, Na^+ ions originating from the SLG scarcely diffused into the device. However, the ions from the perovskite materials such as Br, I, Cs, and Pb exhibited diffusion under the influence of a negative potential, leading to irreversible degradation (Fig. 12(c)). There is a possibility that these elements migrated as negative ion groups, such as CsI and PbBr, due to the strong negative potential. These researchers shed light on the severe consequences of PID on the PVSK/Si TSC, a topic that has been largely overlooked in previous reports. Thus, to address these issues, it may be worth exploring new module designs, such as an encapsulant-free design, given that conventional insulation strategies fail to meet international standards.

In the absence of mechanical support between the module frame and solar cells, the inert environment offers better insulation compared to TPU. To prevent further ion diffusion, it is recommended to deposit a suitable barrier layer between the perovskite layer and the polymeric encapsulating film. Additionally, it is important to employ subcell characterization platforms such as three-terminal characterization platform and subcell selective illumination approaches to gain a deeper understanding of the PID mechanism.[239]

8.7. Metal degradation mechanisms and PID of PSCs

The interaction between different perovskite species and the metal electrode is of utmost importance, given that it represents a decomposition pathway that cannot be prevented by encapsulation. Specific metals have the capability to immediately form a redox couple with the perovskite material or undergo a reaction with PbI_2.[240] Au does not experience a chemical reaction with perovskite, but it reacts with the highly reactive polyiodide melts generated as a result of the disintegration of the perovskite.[241] The majority of metals undergo a reaction with the decomposition products of perovskite. The three-metal electrode reaction pathways can be described as follows: (1) X-site species are generated during the decomposition of perovskite, and then these species migrate towards the metal electrode. This reaction results in the corrosion of the metal electrode and accelerates the decomposition of perovskite. (2) A metal electrode creates a redox couple with Pb^{2+} ions. The perovskite undergoes rapid decomposition, resulting in the formation of metallic Pb. (3) The metal from the electrode can

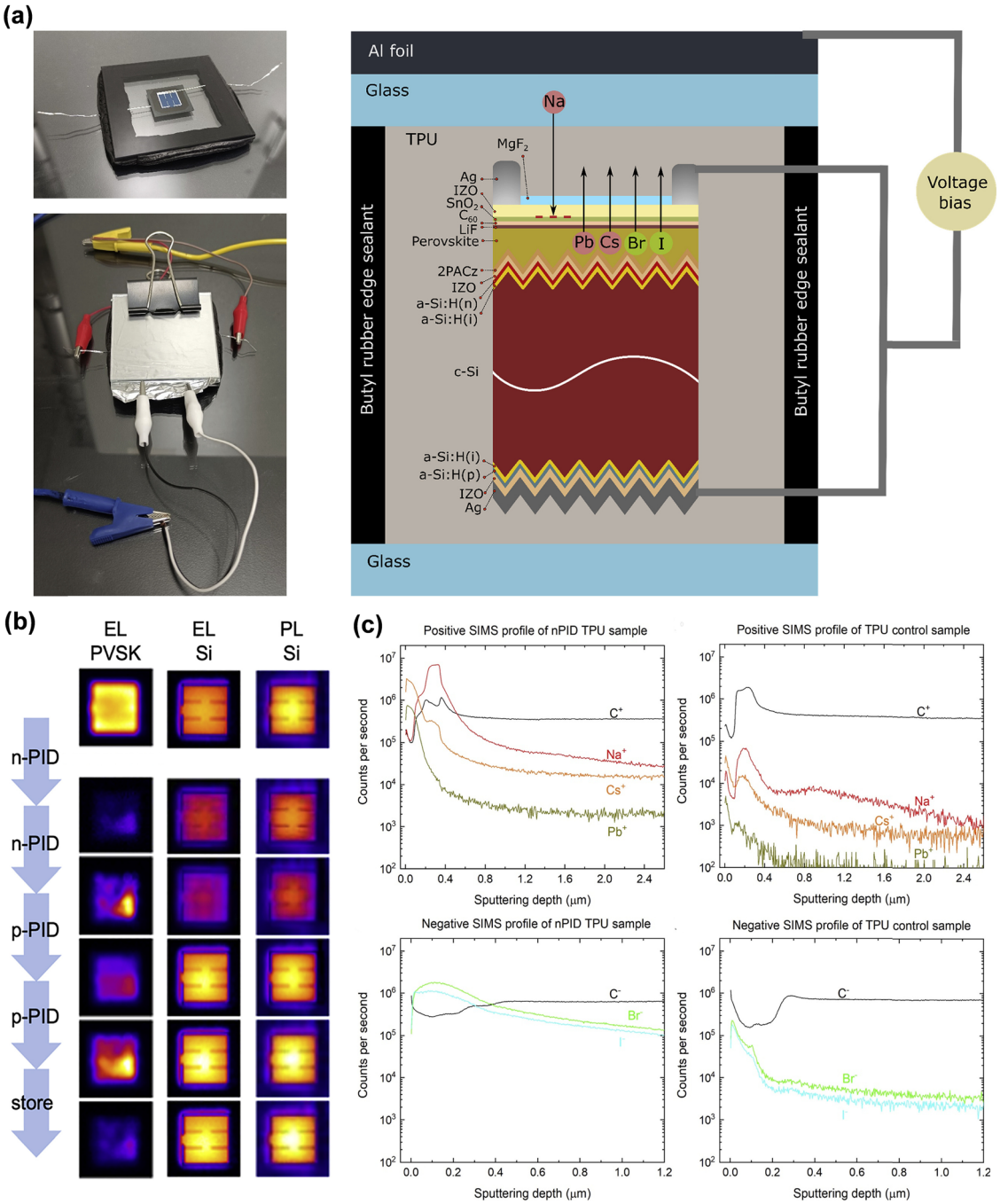

Fig. 12 (a) Encapsulated perovskite/Si tandem mini-modules for the PID experimental setup along with the mini-module structure. Detailed PID analysis of (b) EL and PL scans of the sample at various processing stages. (c) SIMS profile of the n-PID TPU and TPU control samples. The SIMS profile is negative in both the n-PID and control TPU samples. Reproduced with permission.[58] Copyright 2023, Cell Press.

penetrate the perovskite and react with it to generate metal halides, decomposing the perovskite and degrading the metal electrode. Recently, we comprehensively discussed and summarized the role of rear electrode materials, especially metal electrodes, in PSCs.[242]

Only Nakka *et al.*[59] discussed the degradation of the rear electrode under room and elevated temperature conditions in available PID studies of PSCs. The penetration of Ag^+ ions from the rear Ag contact in the perovskite layer and the subsequent development of a strong AgI bond can be observed on the rear surface of the solar cell, both at room temperature and at elevated temperature. The reaction between the I in the perovskite layer and the Ag^+ in the rear electrode results in the formation of AgI, which is a more stable compound compared to bonds such as NaI. Consequently, the AgI peak cannot be reduced, as evidenced by the XRD results, and the devices

showed only partial recovery under room and elevated conditions. Metal-induced degradation becomes relevant in PID studies of PSCs under light and elevated temperature conditions; therefore, it should also be investigated further.

9. Comparison of PID of PSCs, DSSCs, and OPVs

Understanding the process of PID is becoming increasingly important as the solar industry shifts from traditional silicon-based solar cells to cutting-edge third-generation solar cell technologies. This understanding is not confined to traditional silicon-based or thin-film PV but rather encompasses the most recent generation of solar cells, such as PSCs, DSSCs, and highly efficient OPVs. Thus, comprehending PID is crucial for their commercialization and mass production to ensure the long-term efficiency and stable operation of these cutting-edge solar cell technologies under real-world conditions.

Akcaoğlu *et al.*[99] demonstrated a comparison of the voltage and time-dependent PID in PSCs, DSSCs, and OPVs utilizing a bias voltage operation at the cell level. They utilized the concept of exposing the cells to an external potential to study the power degradation in the form of polarization (reversible degradation) and electro-corrosion (irreversible degradation). They exposed their devices to different external voltages under varying light intensities for different durations. To electrochemically examine the PID effect, they conducted *J–V* characterizations, electrochemical impedance spectroscopy (EIS), and external quantum efficiency (EQE) measurement both before and after degradation, under varying light intensities (1–100 mW cm^{-2}) and in the dark. The PSCs were fabricated using the structure of ITO/poly(3,4-ethylenedioxythiophene)polystyrene sulfonate (PEDOT-PSS)/$CH_3NH_3PbI_3$/PCBM/Al, having individual cells with a size of 1089 mm^2 (33 × 33 mm) and with an active area of approximately 0.09 cm^2. After an applied voltage of 3.5 V for 5 min, the device began to degrade, while the cell parameters exhibited an increasing trend. All the measured values followed an increasing trend up to 5 V for 5 min degradation after the cell discharge at the 25th min. After degrading at 5.5 V for 5 min, the device lost 98.4% of its output power relative to the preceding degradation step of 5 V for 5 min. The maximum power output voltage (V_{mp}) was reduced by more than three times and the maximum current density (J_{mp}) was reduced by more than five times, as derived from their original and post-degradation measurements for a total loss of 99.20% in power (PCE dropped to 0.01% from 1.87%). Additionally, the V_{OC} and J_{SC} were found to decline by 420 mV and 9.21 mA cm^{-2}, respectively.

After the initial voltage-dependent degradation test, a second test was conducted. The cell did not discharge during anode-cathode short-circuiting, which is likely because the degradation was stable, and the earlier gain in efficiency did not occur. At the end of the degradation test, the PCE of the cell dropped to 0.07%, representing a total efficiency loss of 98.67%. Additionally, the V_{OC} and V_{mp} decreased by 40 mV and 60 mV, while the J_{SC} and J_{mp} decreased by 13.58 and 5.11 mA cm^{-2}, respectively. Under open circuit conditions, the voltage degradation was relatively small compared to that caused by short circuit conditions. After 25 min, the cell lost 33.82% of its maximum output power compared to the power output recorded after 20 min, and after 25 min, the absolute power loss was slightly less than 50%. An increase in efficiency was observed after applying a 4.5 V bias for 5 min, which can be attributed to the charging capacitance. After 4.5 V bias for 40 min, the PCE degraded from 1.09% to 0.25%, the J_{SC} declined to 6.7 mA cm^{-2}, and there was a 3.63 mA cm^{-2} decrease in J_{mp}. However, there was an improvement in the other parameters, with an increase of 26% for V_{OC}, 47% for V_{mp}, and 69% for FF.

Although the *J–V* characteristics of DSSCs and OPVs were drastically reduced due to voltage-dependent degradation, the PSCs appeared to be the most resistant among the three technologies (Fig. 13(a)). It is important to note that the PSCs showed the lowest efficiency loss of the three technologies examined prior to the degradation tests. As illuminated in Fig. 13(b), the PSCs again proved to be the most resistant to voltage-dependent degradation, and this trend was also reflected in the dark *J–V* characteristics. Fig. 13(a) demonstrates the impacts of time-dependent voltage degradation in *J–V* characteristics, showing that the PSCs degraded after applying a voltage of 4 V. In contrast, the DSSCs could not sustain more than 5 V voltage stress. However, the thermal stress test for the DSSCs at 50–55 °C demonstrated that they are more temperature resistant than PSCs, which degraded significantly at temperatures below 50 °C (Fig. 13(b)). The V_{OC} was relatively steady compared to the J_{SC} across all cases investigated, but especially in the OPVs and DSSCs, suggesting that the J_{SC} loss is the primary cause of power loss. Due to intragrain ion migration, the voltage inside a perovskite grain undergoes significant changes both spatially and temporally after exposure to light. Ion migration causes a residual V_{OC} that varies with time and lasts several minutes, even under dark conditions. This indicates that the electrical properties of the material change locally, both across and within individual grains. However, the voltage dropped temporarily in the dark before gradually returning to its initial level.[243] This behavior is consistent with the fact that it takes some minutes to reach the macroscale equilibrium state due to the time required for trap filling and subsequent ion migration.[244]

The comparison of the EQE-curves of the tested devices (shown in Fig. 14(c)) revealed that the voltage-dependent degradation significantly reduced the efficiency of both the PSCs and DSSCs, while the OPVs performed much better, even when subjected to a voltage bias of 25 V, resulting in only a slight degradation in quantum efficiency.[245] The impact of degradation on the EQE of PSCs resulted in a drop from 60% to 3.5% (Fig. 14(c)), similar to the J_{SC} trend.[246] According to the comparison of the EQE results, the OPVs performed the best regarding voltage degradation, while the PSCs degraded more in both tests. Although PSCs were heated at a lower temperature (42 °C) than DSSCs (55 °C) and OPVs (50 °C), they were

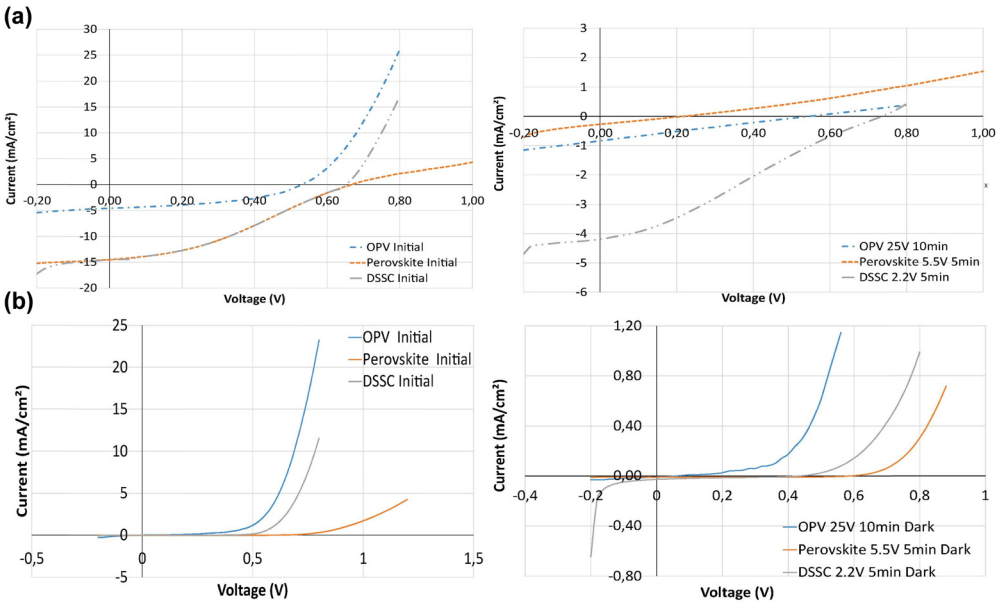

Fig. 13 (a) Illuminated J–V curve comparison reveals voltage-dependent degradation. (b) Comparison of dark J–V curves with voltage-dependent degradation. Reproduced with permission.[99] Copyright 2019, Elsevier.

more vulnerable to temperature-dependent degradation, with an approximate 25% loss of EQE peak. Depending on the temperature, the PSCs degraded differently due to thermal stress. PSCs are known to rapidly lose efficiency when heated to a temperature of 85 °C or higher (which is close to the normal operation under full sunlight). In particular, the reaction between the HTL and the additives during thermal stress is responsible for the PCE drop at low temperatures.[247] Based on these results, it is evident that ion migration and other defects specific to perovskite materials make PSCs more susceptible to thermal degradation than DSSCs and OPVs.

The absolute value of the series resistance remained unchanged in the EIS results of PSCs; however, the parallel resistance increased significantly. Therefore, the voltage-dependent test at 3.5 V for 5 min is the cut-off result, above which the degradation of the PSCs occurred. In the tests lasting less than 20 min, the J_{SC} decreased, while the V_{OC} and FF increased due to the time-dependent degradation. The previously described decrease in charge accumulation at the grain boundaries and the HTL/perovskite interface directly influenced the improved V_{OC} and FF.[248] Fig. 14(d) (voltage-dependent and time-dependent degradation) shows that as PID proceeded, the devices tended to exhibit a higher onset potential and reduced dark current density by enhancing the threshold potential across the energy barrier.[249]

The experimental analysis of the various solar cells revealed that the DSSCs have a limited lifetime under voltage biasing, and the possible manufacturing defects influence their maximum voltage durability. Meanwhile, the PSCs rapidly degraded with a voltage bias higher than 4.5 V, whereas OPVs were physically voltage robust and showed no such degradation even when subjected to a voltage bias of 30 V. Furthermore, to restrain the PID, solar cells must be appropriately connected to a power source when employed on a large scale, given that this will reduce the possibility of irreversible degradation of 3rd generation solar cells.

Finally, to enhance the accuracy and reliability of the findings from the experimental investigation on PSCs, a considerable number of device samples are needed. Therefore, it is suggested that the experimental findings derived from a substantial quantity of device batches can be regarded as reliable. In this case, to ensure the reliability of PSC research, particularly concerning PID, researchers in the PSC community must conduct experiments on a large scale. In addition, numerous companies have entered the emerging field of PV technology. Thus, it is crucial to emphasize using large-area modules manufactured from a scalable production line for conducting PID research.

10. Conclusions and emerging trends

This study aimed to present insight into the latest research carried out recently on PID in PSCs and PSMs, given that these devices are significant for renewable energy applications and commercialization. Considering the importance of PID in the present research, initially, a comprehensive overview on PID was provided, together with its associated mechanisms, methodologies, environmental factors, and testing techniques by focusing on PV technologies that are being widely employed.

The leakage current is considered to be the main cause of PID in PV technologies, which can also be influenced by environmental factors (temperature and humidity), the materials (AR coating, glass, and encapsulating materials), and the system (functional earthing, transformerless or non-isolated inverters, and PV-offset box) or module design. Accordingly, the

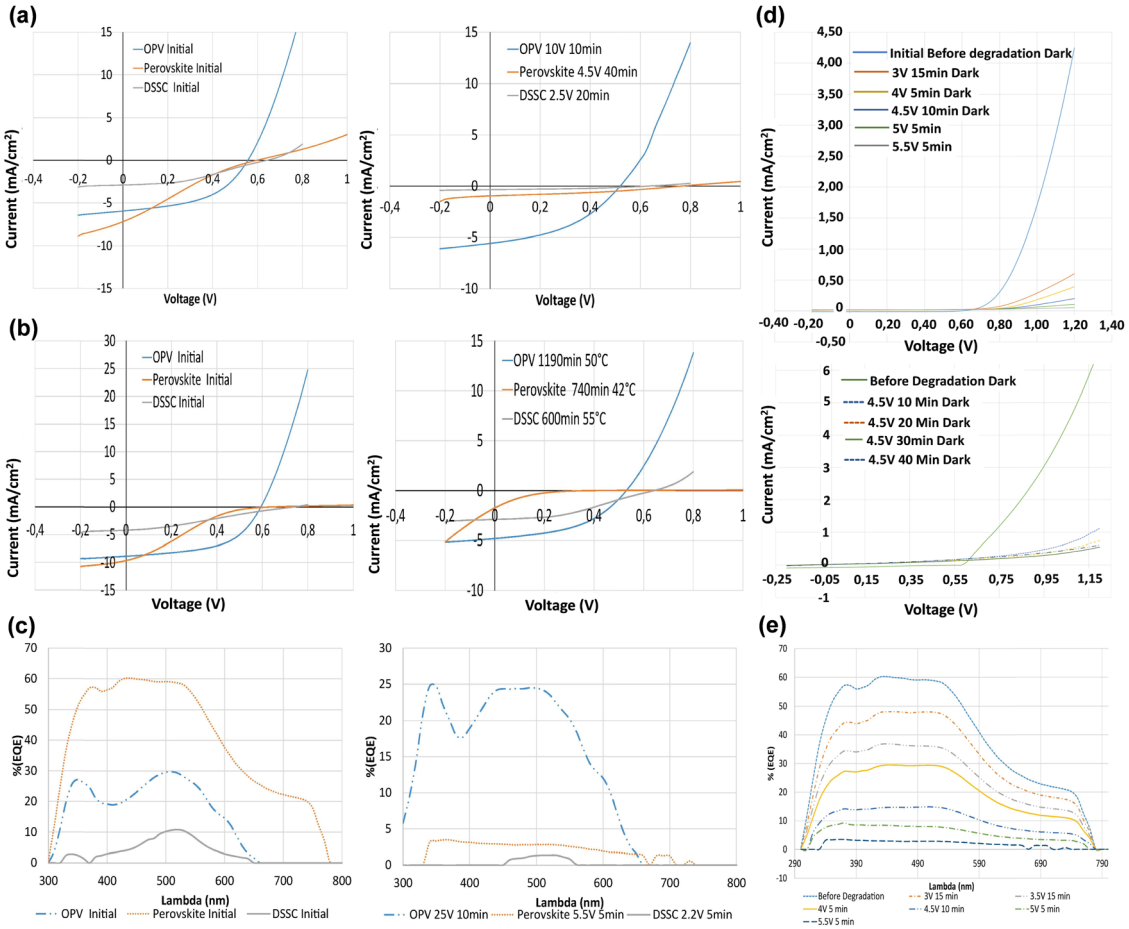

Fig. 14 (a) *J*–*V* curve comparisons revealing time-dependent degradation. (b) Comparison of *J*–*V* curves of temperature-depended degradation. (c) Voltage-dependent degradation comparison *via* EQE curves. (d) PSC voltage-dependent degradation and time-dependent degradation of dark *J*–*V* curves. (e) PSC voltage-dependent degradation presented by EQE curves. Reproduced with permission.[99] Copyright 2019, Elsevier.

research discussed herein provides insight into the different leakage current pathways when the grounded frame and the terminals of the PV modules are subjected to a high voltage. PID tends to switch modes when the same types of PV modules are subjected to different environmental stresses, and therefore various mechanisms are available and discussed herein. Mainly, these mechanism include PID-shunting type, polarization-type PID, and corrosion-type PID. Specifically, the PID-shunting type is found in the conventional p-type c-Si PV modules, the polarization-type PID is found in n-type Si PV modules of PERT, PERL, TOPCon, and IBC devices, including IBC devices with front-floating emitters, and the corrosion-type PID is found in p-type c-Si cell modules and thin-film PV modules. However, further research is needed to identify the exact mechanisms that can adequately explain all PID-related effects. In this pursuit, thin-film-based solar modules are also susceptible to PID due to the electrochemical degradation of their TCO layer, n-type c-Si solar modules are prone to PID due to the surface polarization effect, and normal p-type c-Si solar modules are prone to PID due to PID-shunting. Na^+ migration is a critical factor in developing PID, which is valid for almost every type of solar cell containing SLG, and its accumulation in Si-based and thin-film solar modules may cause several forms of PID. To date, four different types of tests or methods are being used to verify the susceptibility of a cell or module to PID. Modules are tested with strategies such as the climate chamber and Al or Cu foil methods. In contrast, devices exhibiting PID sensitivity can be investigated by the corona discharge assembly method or applying a bias voltage to a layer stack that resembles a module.

Subsequent to the discussion provided on PID in PV technologies, a concise and systematic survey related to the research carried out on PID in PSCs was provided, which revealed that certain challenges, in commercializing PSCs, need to be addressed. These challenges include the exposure of devices to environmental stresses such as light, heat, moisture, oxygen, and electric field during actual field operation and applications.

PSCs are in the development stage and require proper standardized test protocols, and therefore, available test protocols applied to PV technologies are being used. However, studies and experiments revealed that by applying these protocols, the sustainability of the cells for longer durations have been compromised, given that PID is widely acknowledged to

be one of the reliability threats because of which the cells are likely to be affected within a minimal timeframe. Moreover, it has been established that PSCs are susceptible to PID. In this case, the IEC 62876 and IEC61215 standards are equally important in dealing with PID in solar cells, particularly in providing effective solutions for alleviating PID in PSCs due to their particular ion migration phenomena, which distinguishes them from other PV technologies.[250] Considering the importance of the stability of the PSCs, researchers found that PID is a stability concern that can significantly affect large-scale installations. When a negative bias is applied, Na^+ migrates through glass layers and into cells, causing undesirable degradation. Similar to that observed in other PV technologies. In addition, a depth profile and imaging using ToF-SIMS indicated that Na^+ was abundant in the negatively biased devices. The PID predominantly impacted the perovskite/silicon tandems in the perovskite top subcell. The PID of PSCs can be recovered or partially recovered by exposing the negatively biased device to a positive bias, which forces the Na^+ from the active layers back to the glass by reversing the penetration of Na^+. The published results to date suggest that PSCs are particularly vulnerable to PID given that the elements diffuse out of the perovskite under a high electric field. Thus, to compete with other PV technologies for a commercial market share, PSCs must satisfy or exceed the basic requirements.

Based on recent studies, PID has been identified as a critical stability issue for both conventional Si-based solar cells and PSCs, hampering their mainstream application in the PV technology industry. Thus, to facilitate the commercialization of PID-free or less affected perovskite PV technologies, the following suggestions are proposed:

• Further research is needed to understand the mechanisms, mitigation techniques, and kinetics of PID in PSCs. This research should consider the structural and compositional variations in PSCs.

• Environmental stressors can be mitigated through the use of various encapsulation methods. Exploring different encapsulation methodologies can help to protect PSCs from the detrimental effects of PID.

• Introducing an interlayer between the SLG and cell can minimize the migration of Na^+ ions, which is a critical factor in PID. This approach is likely to overcome the effects of PID in PSCs.

• Considering the versatile characteristics and degradation mechanisms associated with PSCs, standardized testing protocols can be established for PSCs to accurately investigate their susceptibility to PID. This will enable reliable and consistent evaluation of PID resistance in different PSC technologies.

• Novel and innovative techniques need to be developed to mitigate or eliminate the effects of PID in PSCs. These techniques may include but are not limited to the use of advanced encapsulation materials, interlayers, and other engineering solutions such as the replacement of the A, B, and X sites with some stable materials that can block Na^+ ion penetration, employing Na-free front glass, and introducing some inorganic and interactive transparent layer between the glass and transparent electrode, which can considerably reduce the impact of PID on PSC.

• Flexible solar cells/modules can be utilized to reduce PID given that many of the flexible substrates are either glass-free or made of ultrathin glass with minimal Na content.

Overall, the comprehensive review provided in this study serves as a valuable resource for the research community devoted to investigating and addressing the PID phenomenon in PSCs, ultimately paving the way for their successful commercialization.

Author contributions

Conceptualization, W. C., H. R. and Z. L.; investigation, H. R., Z. L. and W. C.; project administration, W. C., Z. L., and Z. Y.; writing – original draft, H.R.; writing – review and editing, H. R., T. M., Y. G., M. A., M. Y., S. L, and J. W. All authors have read and agreed to the published version of the manuscript.

Conflicts of interest

The authors declare no conflict of interest.

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